30V Half Bridge Dual N-Channel Super Trench Power MOSFET

Description

The MJXPB303GU uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. It includes two specialized MOSFETs in a dual Power DFN5x6 package.

General Features

Q1 "High Side" MOSFET

- V_{DS}=30V,I_D=30A
  $R_{DS(ON)}$ <5.8mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <8.9mΩ @ V_{GS}=4.5V

Q2 "Low Side" MOSFET

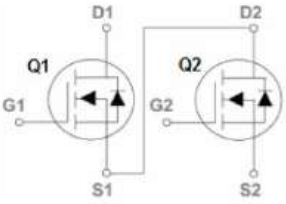
- V_{DS}=30V,I_D=100A
  $R_{DS(ON)}$ <1.9mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <2.8mΩ @ V_{GS}=4.5V

- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150°C operating temperature
- Pb-free lead plating
- RoHS compliant
- Halogen free

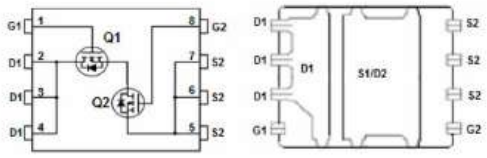
Application

- Compact DC/DC converter applications

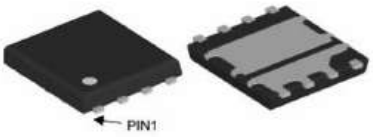
100% UIS TESTED! 100% ΔVds TESTED!



Schematic Diagram



pin assignment



Top View Bottom View

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
PB303GU	MJXPB303GU	DFN5X6-8L	330mm	12mm	5000 units

Absolute Maximum Ratings (T_C =25℃ unless otherwise noted)

Parameter		Symbol	Q1	Q2	Unit
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current (Note 2)	T_C=25°C	I_D	30	100	A
	T_C=100°C	I_D	21	70	A
Drain Current -Pulsed (Note 1)		I_{DM}	120	400	A
Power Dissipation	T_C=25°C	P_D	30	80	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	-55 To 150	℃

Thermal Characteristic

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance,Junction-to-Case (Note 2) (Q1)	$R_{\theta JC}$	3.3	4.2	℃/W
Thermal Resistance,Junction-to-Case (Note 2) (Q2)	$R_{\theta JC}$	1.2	1.6	℃/W

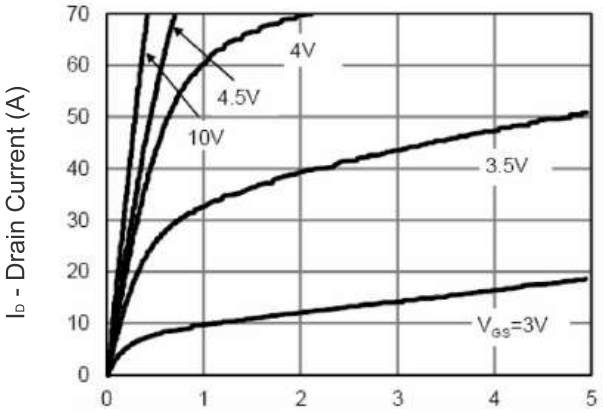
Q1 Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=15A	-	5.2	5.8	mΩ
		V_{GS}=4.5V,I_D=15A	-	7.7	8.9	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=15A	-	30	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V F=1.0MHz	-	822	-	PF
Output Capacitance	C_{oss}		-	344	-	PF
Reverse Transfer Capacitance	C_{rss}		-	15.3	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,I_D=15A V_{GS}=10V,R_G=1.6Ω	-	6.5	-	nS
Turn-on Rise Time	t_r		-	2.5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	nS
Turn-Off Fall Time	t_f		-	2.5	-	nS
Total Gate Charge	Q_g	V_{DS}=15V,I_D=15A V_{GS}=10V	-	15	-	nC
Gate-Source Charge	Q_{gs}		-	2.9	-	nC
Gate-Drain Charge	Q_{gd}		-	2.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	30	A
Reverse Recovery Time	t_{rr}	T_J=25°C,I_F= I_S di/dt= 100A/μs (Note 3)	-	11	-	nS
Reverse Recovery Charge	Q_{rr}		-	19	-	nC

Notes:

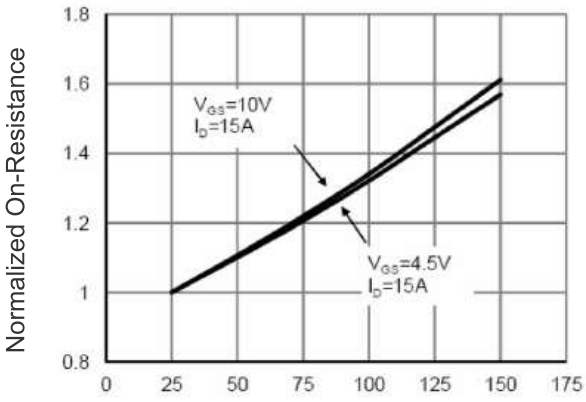
① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition : T_J=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω

Q1 Typical Electrical and Thermal Characteristics



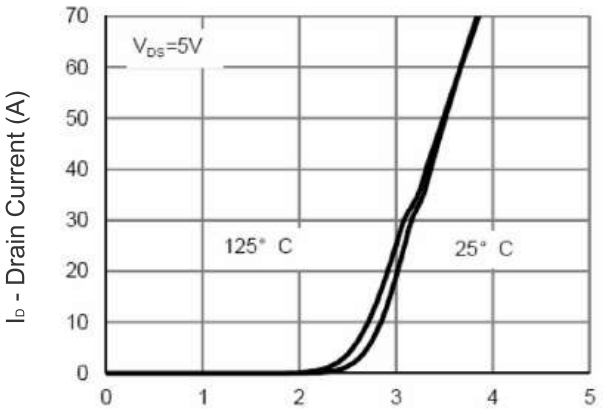
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



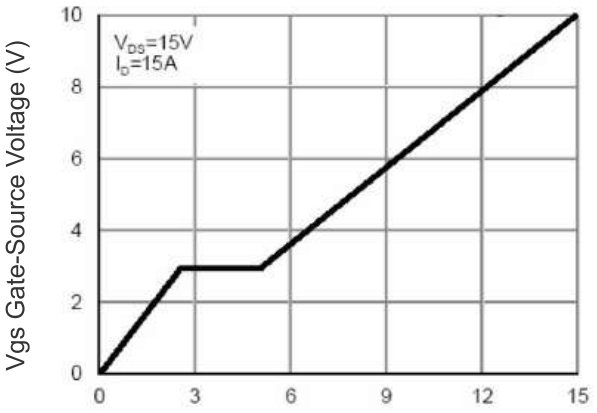
T_J-Junction Temperature (°C)

Figure 4 Rdson-Junction Temperature



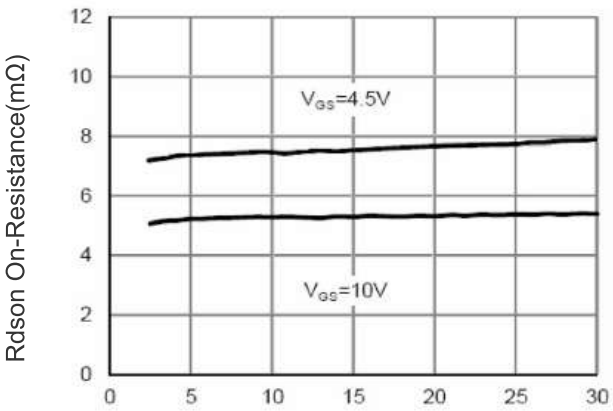
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



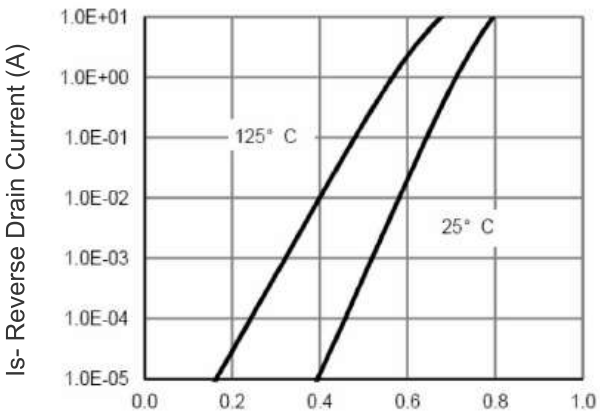
Qg Gate Charge (nC)

Figure 5 Gate Charge



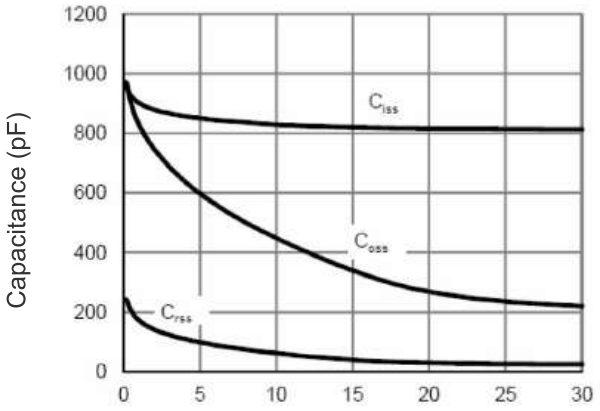
I_D - Drain Current (A)

Figure 3 Rdson- Drain Current



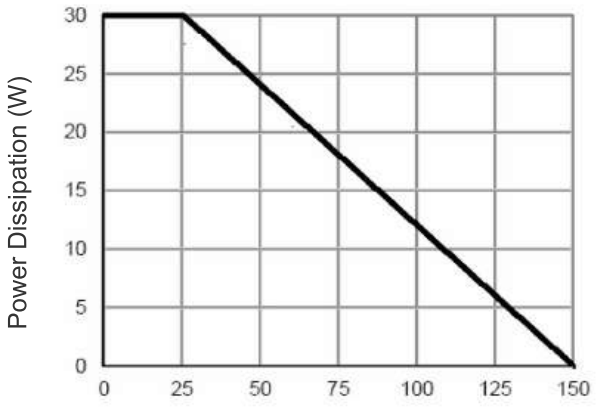
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



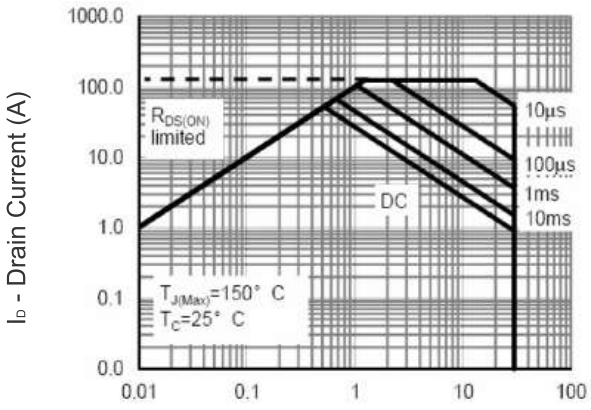
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



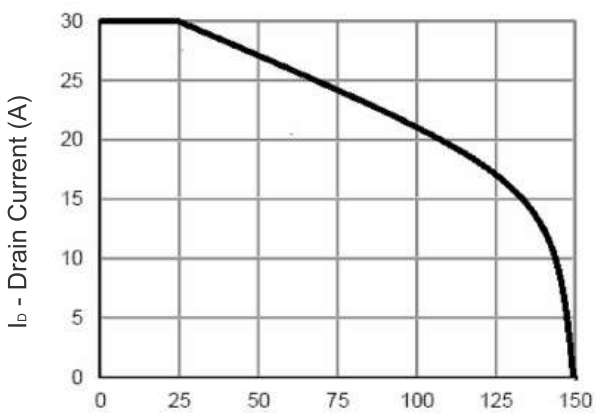
Tc-Case Temperature(℃)

Figure 9 Power De-rating



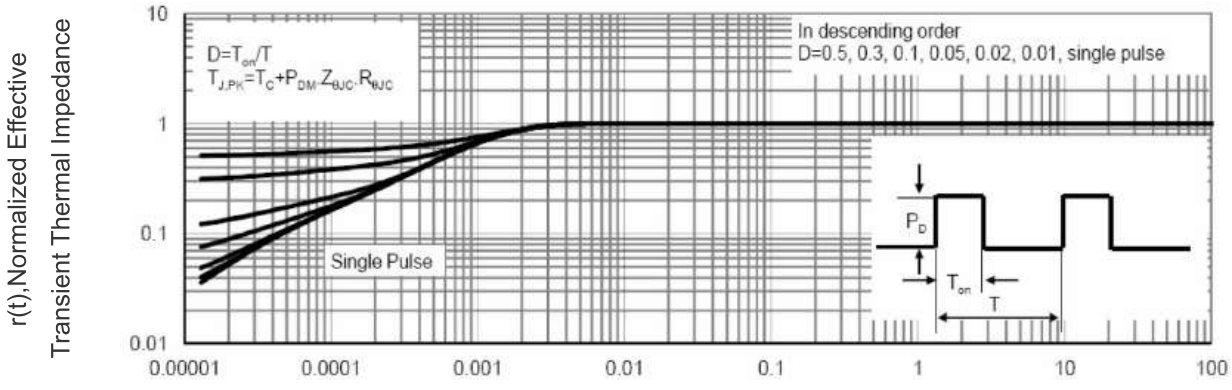
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tc-Case Temperature(℃)

Figure 10 Current De-rating



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

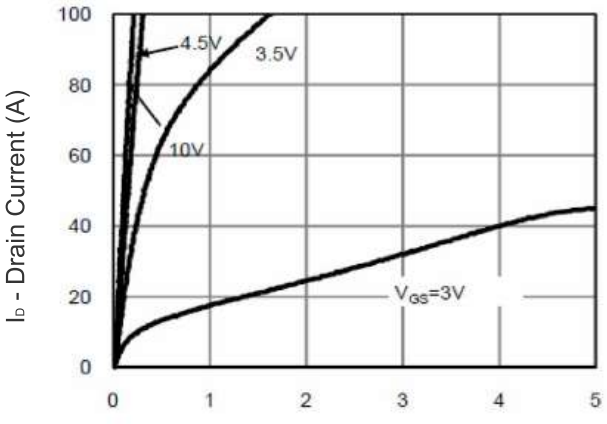
Q2 Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.7	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A	-	1.7	1.9	mΩ
		V_{GS}=4.5V,I_D=50A	-	2.4	2.8	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=50A	-	65	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V F=1.0MHz	-	3370	-	PF
Output Capacitance	C_{oss}		-	902	-	PF
Reverse Transfer Capacitance	C_{rss}		-	60	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,I_D=50A V_{GS}=10V,R_G=1.6Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	nS
Turn-Off Fall Time	t_f		-	9	-	nS
Total Gate Charge	Q_g	V_{DS}=15V,I_D=50A V_{GS}=10V	-	55	-	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain Charge	Q_{gd}		-	8.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=50A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	100	A
Reverse Recovery Time	t_{rr}	T_J=25°C,I_F= I_S di/dt= 500A/μs (Note 3)	-	20	-	nS
Reverse Recovery Charge	Q_{rr}		-	50	-	nC

Notes:

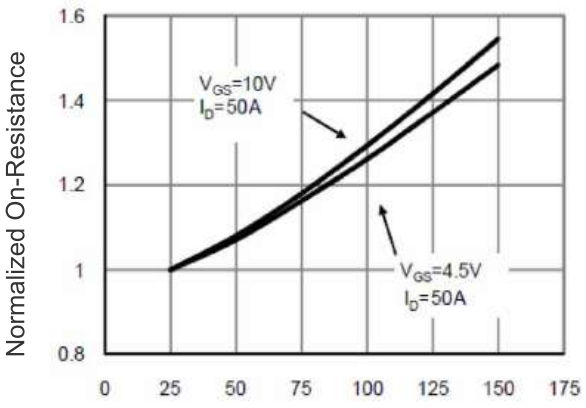
① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition : T_J=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω

Q2 Typical Electrical and Thermal Characteristics



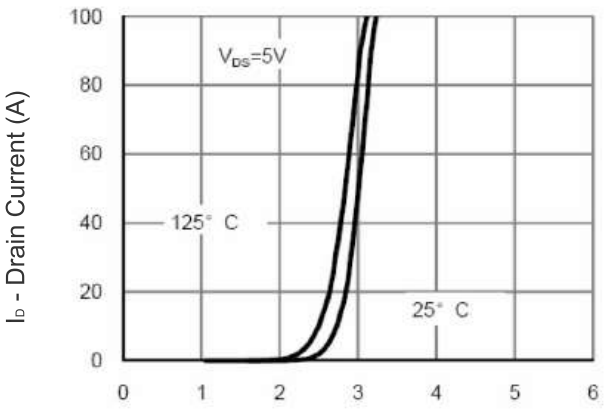
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



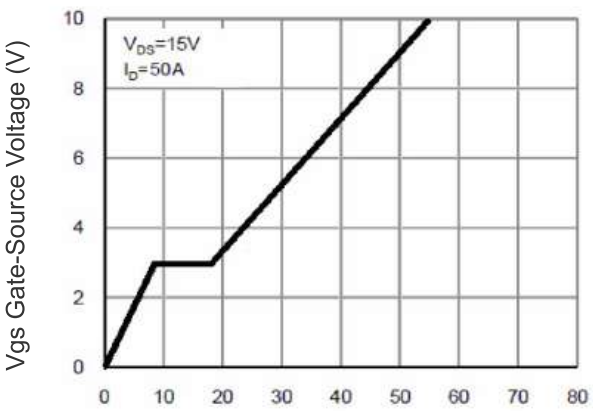
TJ-Junction Temperature (°C)

Figure 4 Rdson-Junction Temperature



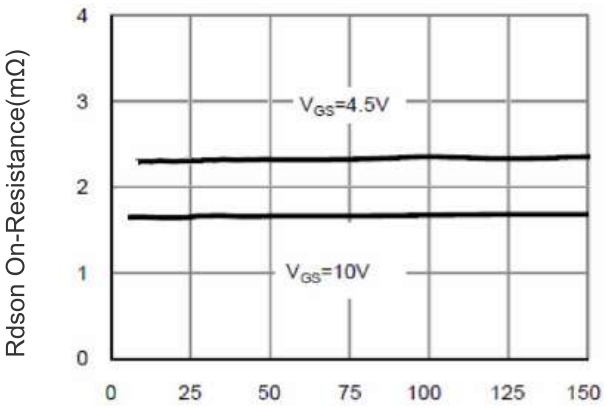
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



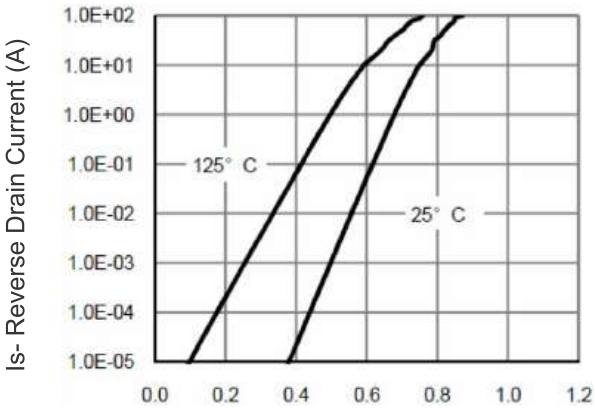
Qg Gate Charge (nC)

Figure 5 Gate Charge



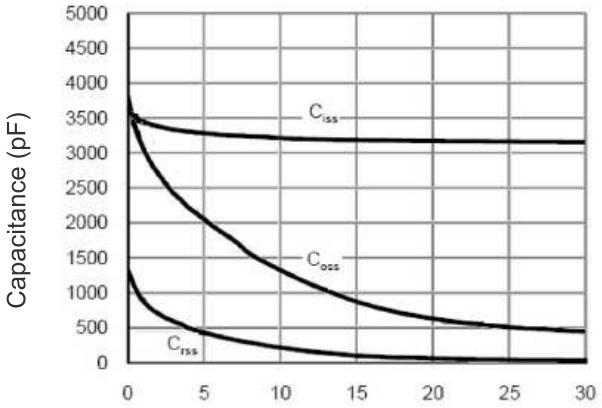
ID - Drain Current (A)

Figure 3 Rdson- Drain Current



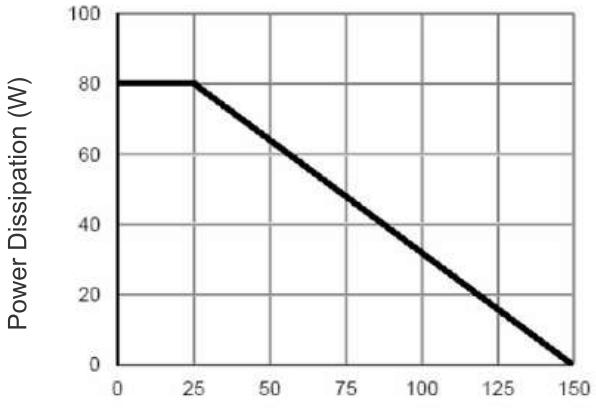
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



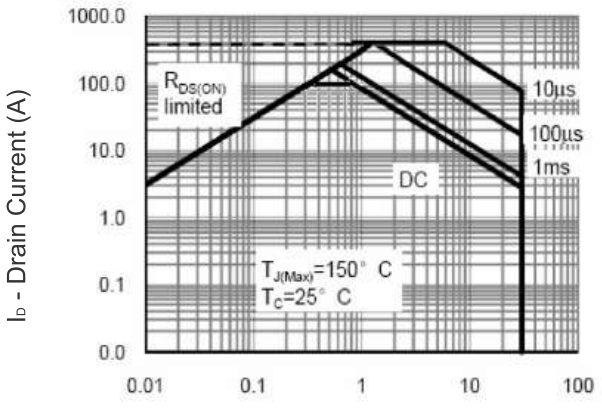
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



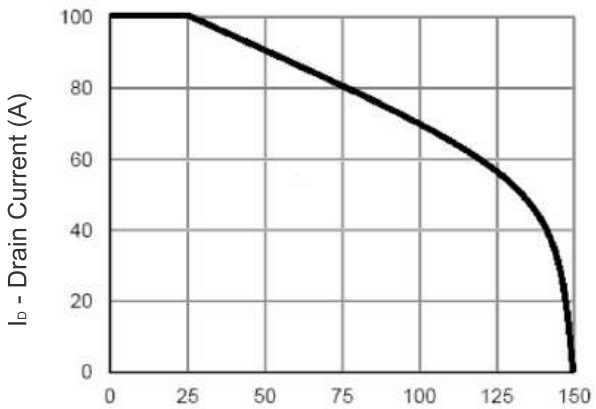
T_{Case}-Junction Temperature(℃)

Figure 9 Power De-rating



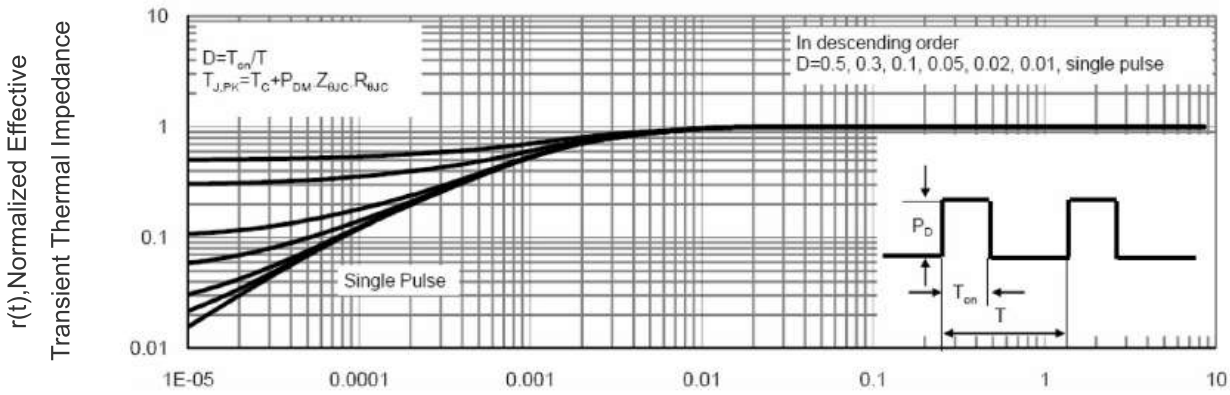
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



T_C-Case Temperature(℃)

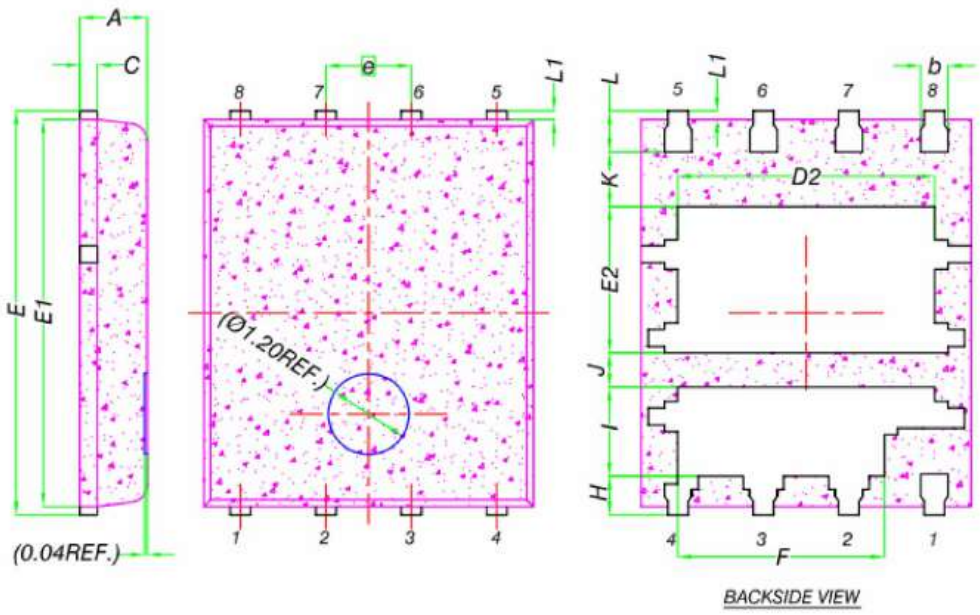
Figure 10 Current De-rating

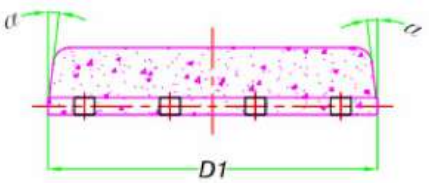


Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

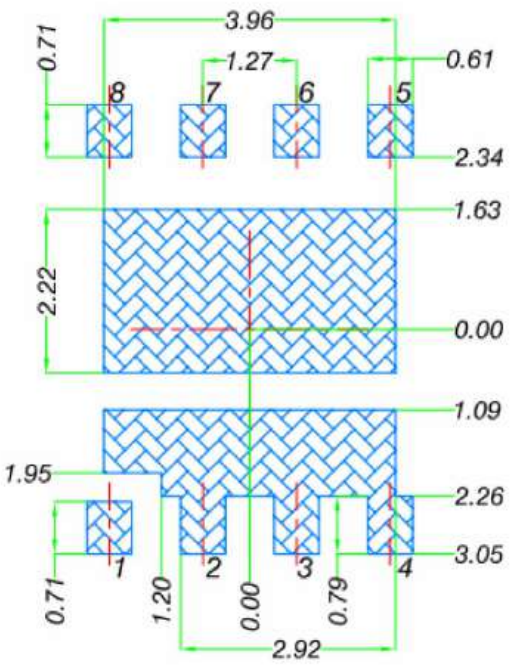
DFN5X6-8L Package Information

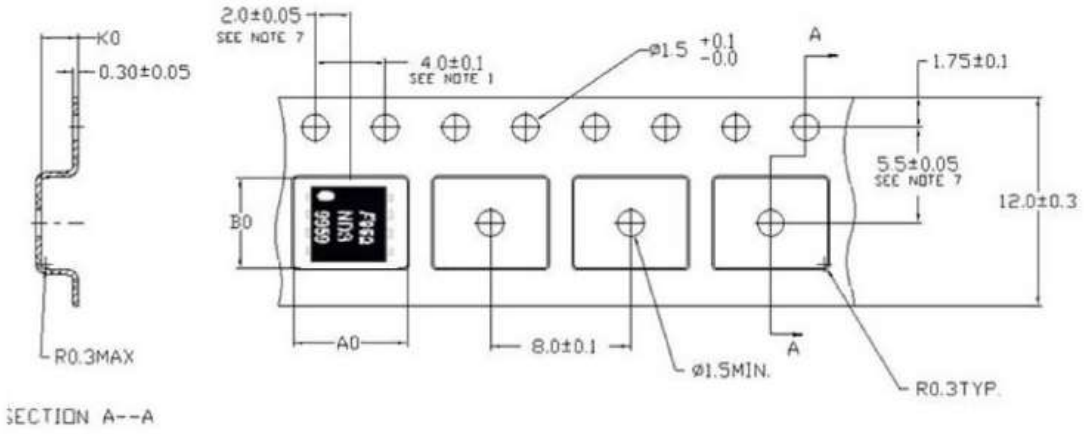




DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	2.02	2.17	2.32
e	1.27 BSC		
F	2.87	3.07	3.22
H	0.48	0.58	0.68
I	1.22	1.32	1.42
J	0.40	0.50	0.60
K	0.50	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

Land Pattern
(Only for Reference)




K0
0.30±0.05
R0.3MAX
SECTION A--A
2.0±0.05
SEE NOTE 7
4.0±0.1
SEE NOTE 1
ø1.5 +0.1 -0.0
A
1.75±0.1
5.5±0.05
SEE NOTE 7
12.0±0.3
B0
A0
8.0±0.1
ø1.5MIN.
R0.3TYP.

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MJ power Semiconductor CO.,LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

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