MJ N-Channel Super Trench Power MOSFET

Description

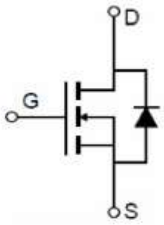
The MJXP60T15AG uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

General Features

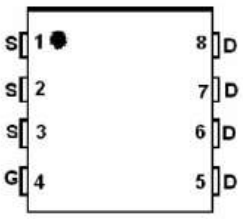
- V_{DS}=60V,I_D=150A
  $R_{DS(ON)}$ < 3.0mΩ @ V_{GS}=10V (Typ:2.7mΩ)
  $R_{DS(ON)}$ < 3.3mΩ @ V_{GS}=4.5V (Typ:2.9mΩ)
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150°C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

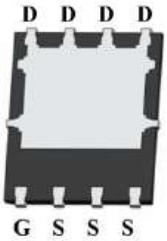


Schematic Diagram



Marking and pin assignment

Top View



Bottom View

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJXP60T15AG	MJXP60T15AG	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous (Silicon Limited)	I_D	150	A
Drain Current-Continuous (T_C =100℃)	$I_{D(100℃)}$	105	A
Pulsed Drain Current	I_{DM}	600	A
Maximum Power Dissipation	P_D	200	W
Derating factor		1.6	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	819	mJ
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.625	℃/W

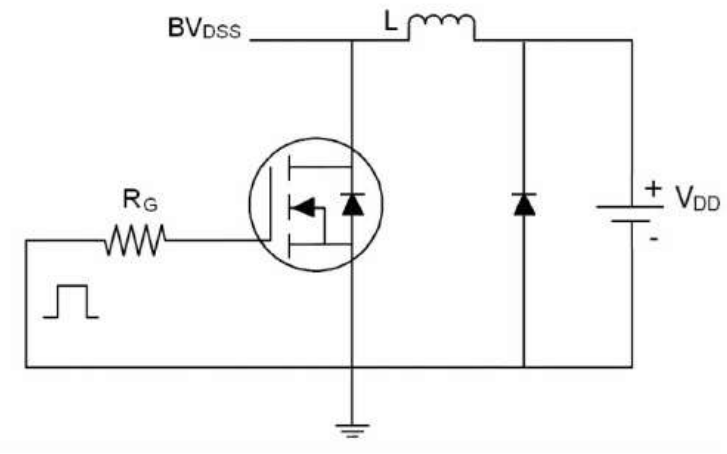
Electrical Characteristics (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.8	2.4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=20A	-	2.7	3.0	mΩ
		V_{GS}=4.5V,I_D=20A	-	3.1	3.5	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	50	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V F=1.0MHz	-	5500	5900	PF
Output Capacitance	C_{oss}		-	955	1000	PF
Reverse Transfer Capacitance	C_{rss}		-	25	30	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=75A V_{GS}=10V,R_G=4.7Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	nS
Turn-Off Fall Time	t_f		-	4	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=75A V_{GS}=10V	-	88	98	nC
Gate-Source Charge	Q_{gs}		-	13	15	nC
Gate-Drain Charge	Q_{gd}		-	14	16	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=150A	-	-	1.2	V
Diode Forward Current	I_S		-	-	150	A
Reverse Recovery Time	t_{rr}	T_J=25°C,I_F= I_S di/dt= 100A/μs (Note 3)	-	56	-	nS
Reverse Recovery Charge	Q_{rr}		-	80	-	nC

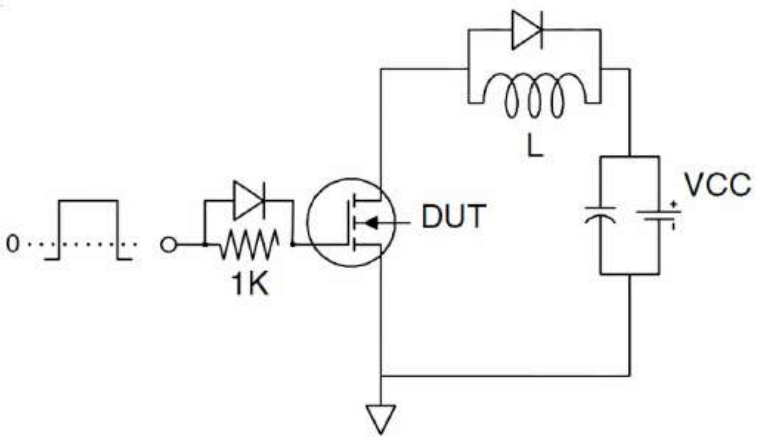
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition : T_j=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

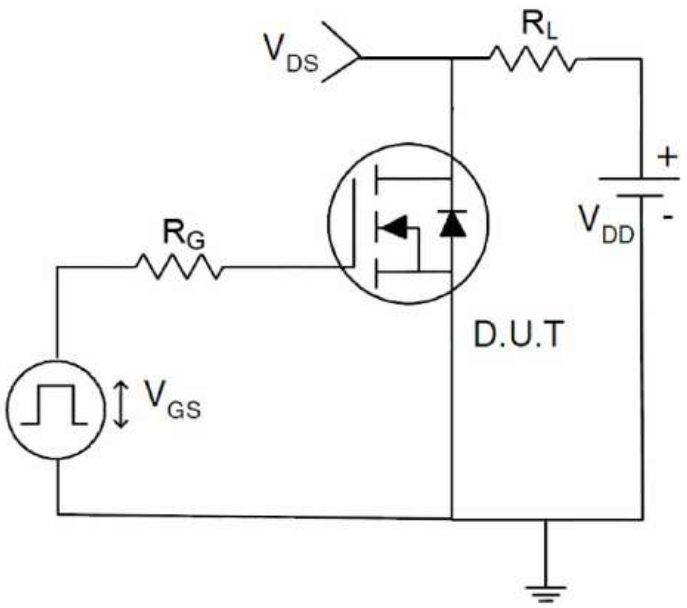
Test circuit



EAS test Circuit



Gate charge test Circuit



Switch Time Test Circuit

Typical Electrical and Thermal Characteristics

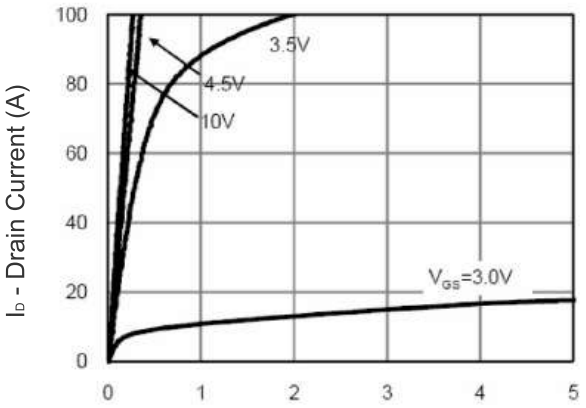


Figure 1 Output Characteristics

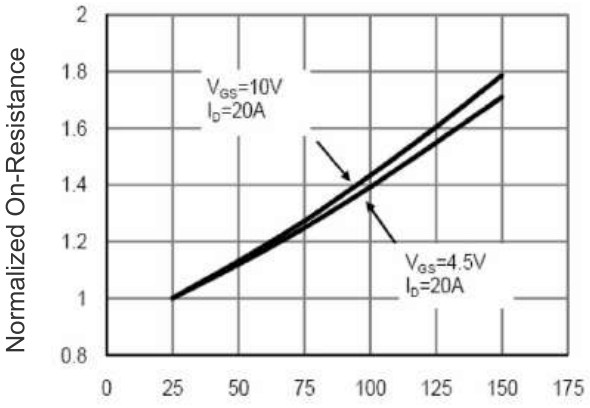


Figure 4 Rdson-Junction Temperature

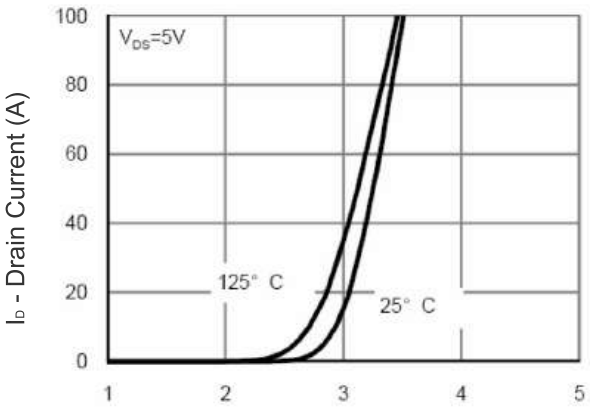


Figure 2 Transfer Characteristics

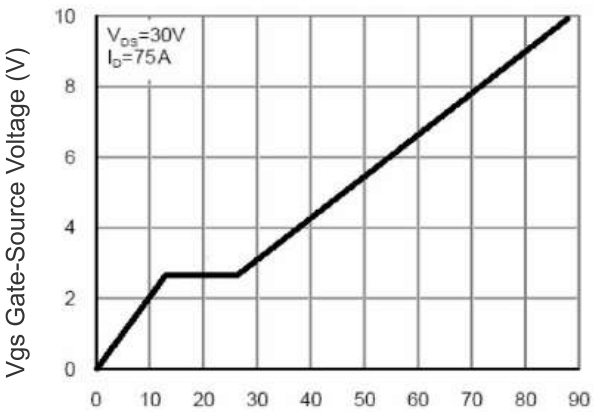


Figure 5 Gate Charge

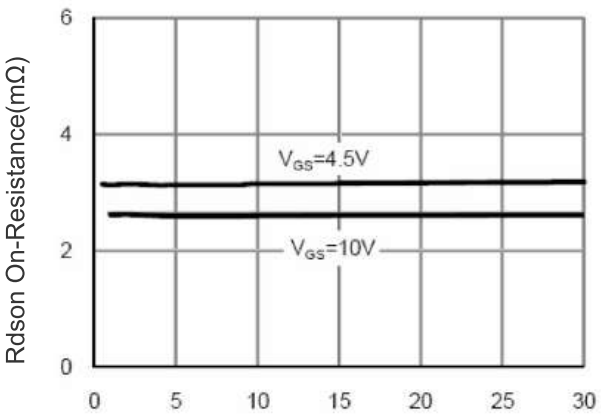


Figure 3 Rdson- Drain Current

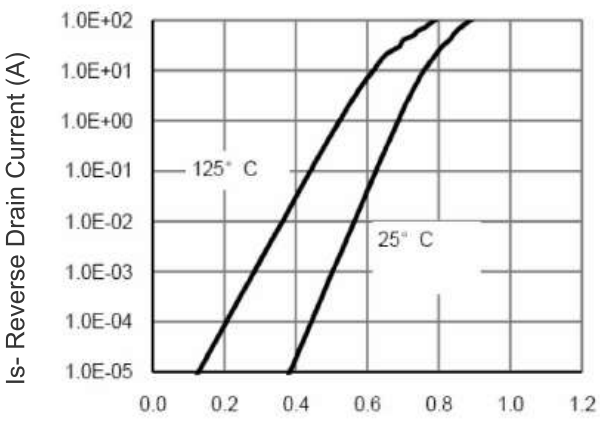


Figure 6 Source- Drain Diode Forward

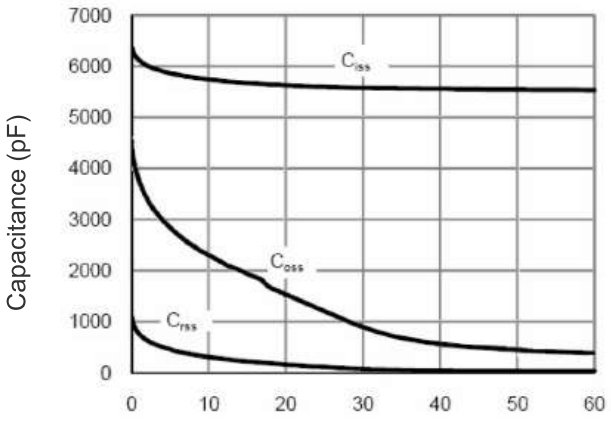


Figure 7 Capacitance vs Vds

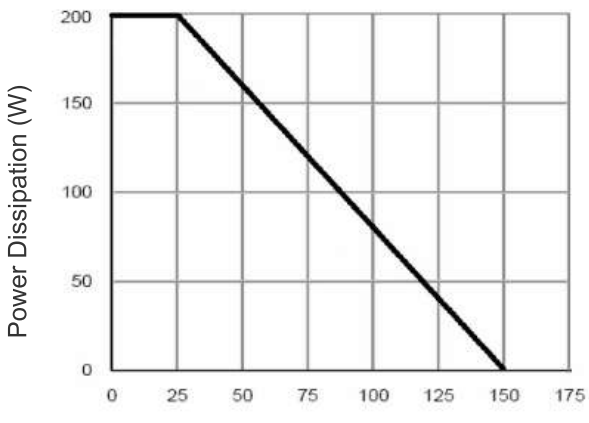


Figure 9 Power De-rating

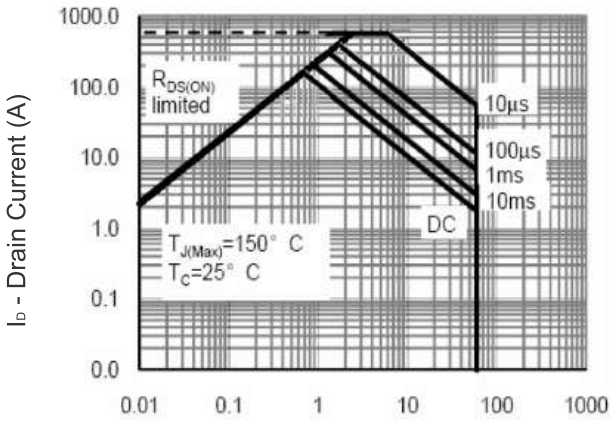


Figure 8 Safe Operation Area

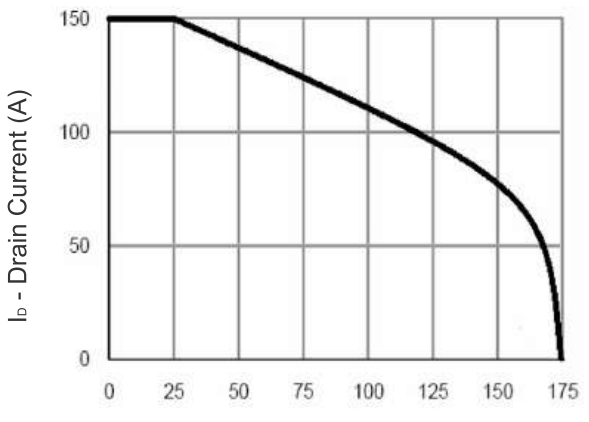


Figure 10 Current De-rating

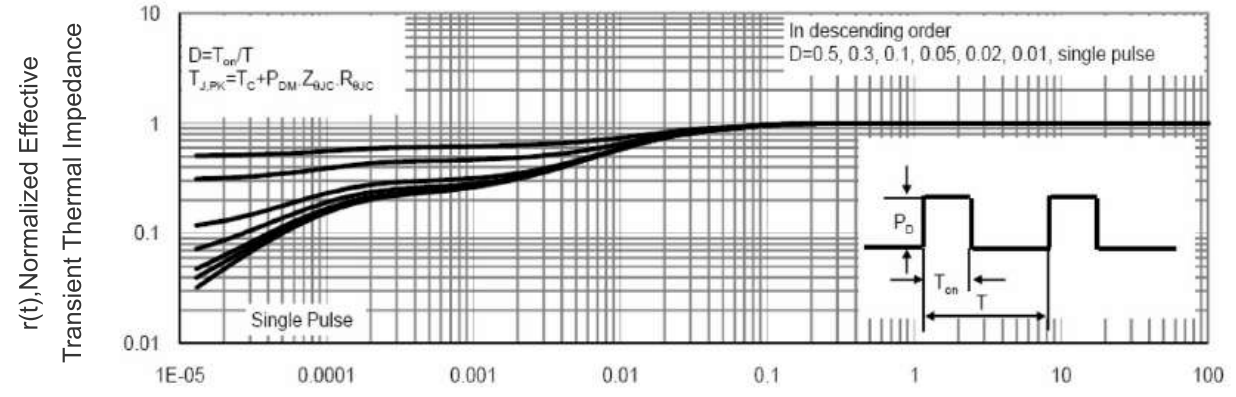
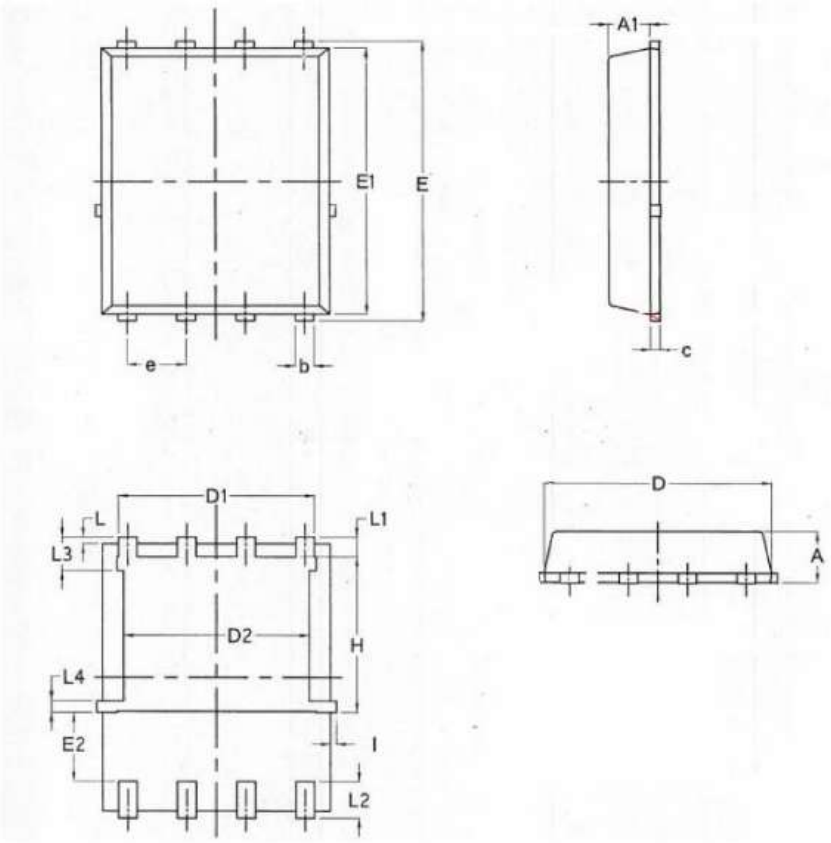


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.90	1.10	1.17	0.0354	0.0433	0.0461
A1	0.824	0.897	0.97	0.0324	0.0353	0.0382
b	0.33	0.41	0.50	0.0130	0.0161	0.0197
C	0.150	0.20	0.250	0.0059	0.0079	0.0098
D	4.80	4.90	5.00	0.1890	0.1929	0.1969
D1	3.91	4.22	4.36	0.1539	0.1661	0.1717
D2	3.85	4.00	4.15	0.1516	0.1575	0.1634
E	5.90	60.5	6.15	0.2323	0.2382	0.2421
E1	5.65	5.76	5.85	0.2224	0.2268	0.2303
E2	1.10	/	/	0.0433	/	/
e	1.27 BSC			0.050 BSC		
L	0.05	0.15	0.25	0.0020	0.0059	0.0098
L1	0.38	0.425	0.50	0.0150	0.0167	0.0197
L2	0.51	0.785	0.86	0.0201	0.0309	0.0339
L3	0.55	0.70	0.85	0.0217	0.0276	0.0335
L4	0.10	0.25	0.40	0.0039	0.0098	0.0157
H	3.25	3.35	3.58	0.1280	0.1319	0.1409
I	0	/	0.18	0	/	0.0071

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