

MJ N-Channel Super Trench Power MOSFET

Description

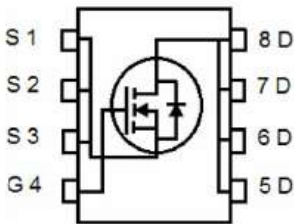
The MJXP1250AG uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- ◆ $V_{DS}=120V, I_D=50A$
 $R_{DS(ON)}=10m\Omega$ (typical) @ $V_{GS}=10V$
 $R_{DS(ON)}=12m\Omega$ (typical) @ $V_{GS}=4.5V$
- ◆ Excellent gate charge x $R_{DS(ON)}$ product(FOM)
- ◆ Very low on-resistance $R_{DS(on)}$
- ◆ 150°C operating temperature
- ◆ Pb-free lead plating

Application

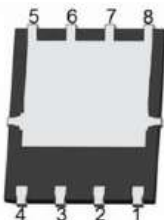
- ◆ DC/DC Converter
- ◆ Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View



Bottom View

DFN 5X6

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJXP1250AG	MJXP1250AG	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_{D(100^{\circ}C)}$	35.4	A
Pulsed Drain Current (Note 1)	I_{DM}	200	A
Maximum Power Dissipation	P_D	80	W
Derating factor		0.64	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	300	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	1.56	°C/W
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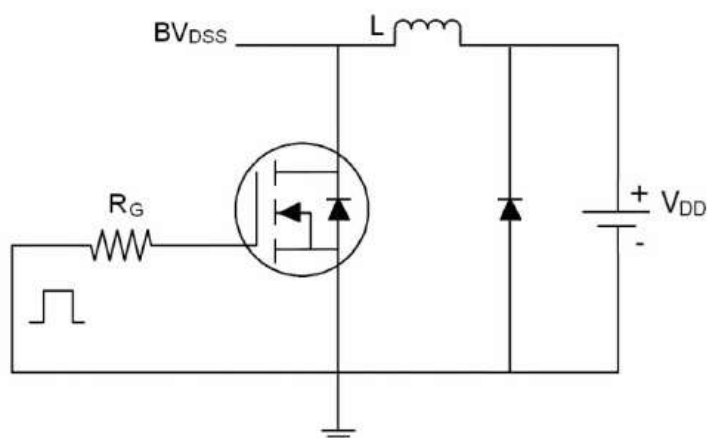
Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	120	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =120V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.0	1.7	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	10	11.5	mΩ
		V _{GS} =4.5V, I _D =20A	-	12	15	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =20A	-	30	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =60V,V _{GS} =0V F=1.0MHz	-	2500	-	PF
Output Capacitance	C _{oss}		-	273	-	PF
Reverse Transfer Capacitance	C _{rss}		-	27	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V,I _D =20A V _{GS} =10V,R _G =3Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	7.5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	26	-	nS
Turn-Off Fall Time	t _f		-	4	-	nS
Total Gate Charge	Q _g	V _{DS} =60V,I _D =20A V _{GS} =10V	-	37	-	nC
Gate-Source Charge	Q _{gs}		-	14	-	nC
Gate-Drain Charge	Q _{gd}		-	8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	50	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =I _S di/dt=100A/μs <small>(Note 3)</small>	-	58	-	nS
Reverse Recovery Charge	Q _{rr}		-	149	-	nC

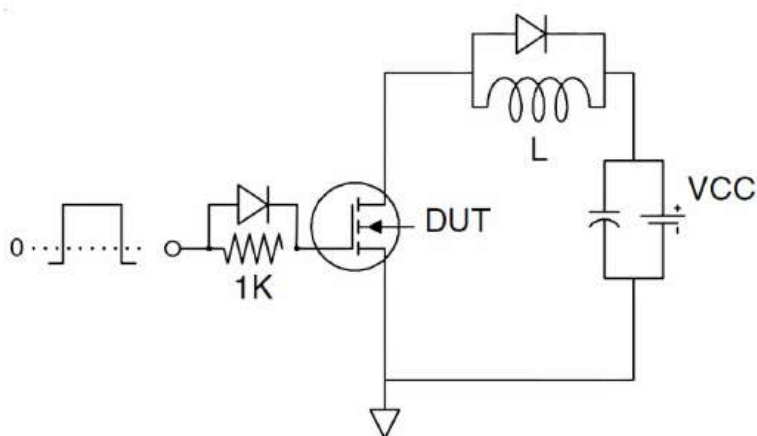
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C,V_{DD}=50V,V_G=10V,L=0.5mH,R_G=25Ω

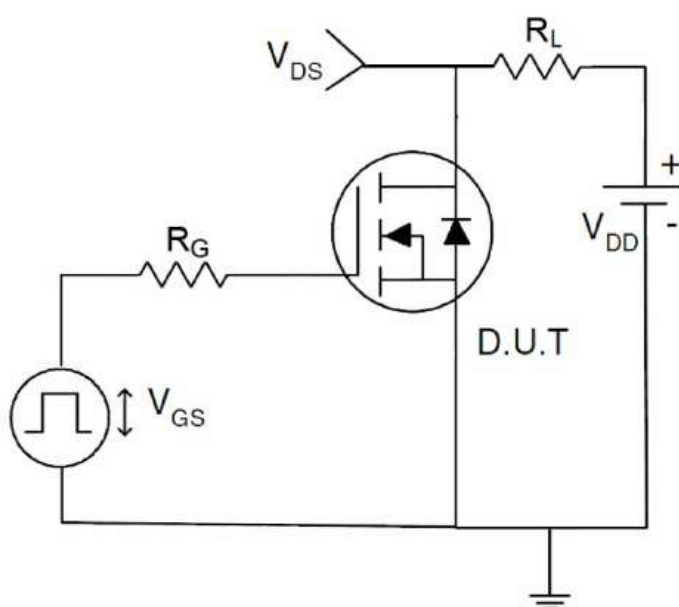
Test circuit



EAS test Circuit

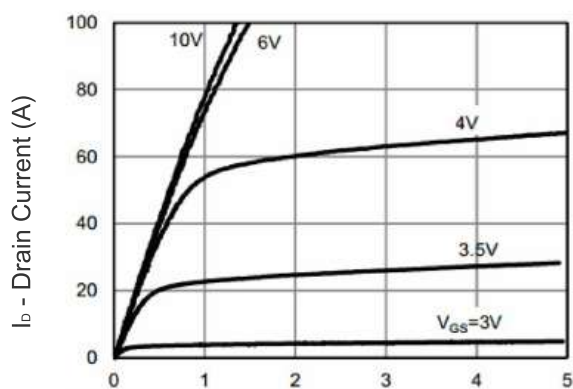


Gate charge test Circuit



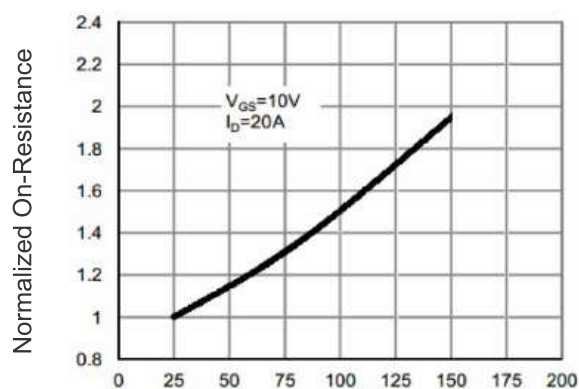
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics



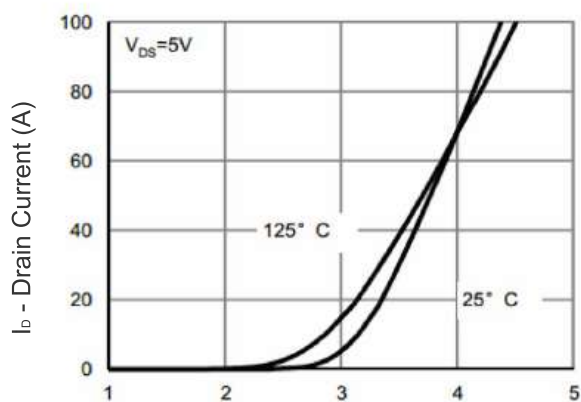
V_{DS} Drain-Source Voltage (V)

Figure 1 Output Characteristics



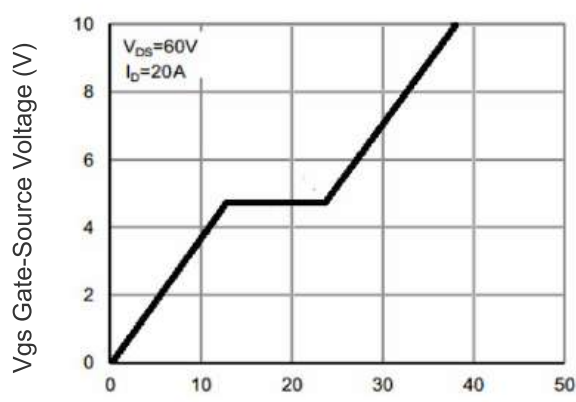
T_J -Junction Temperature($^{\circ}$ C)

Figure 4 $R_{DS(on)}$ -Junction Temperature



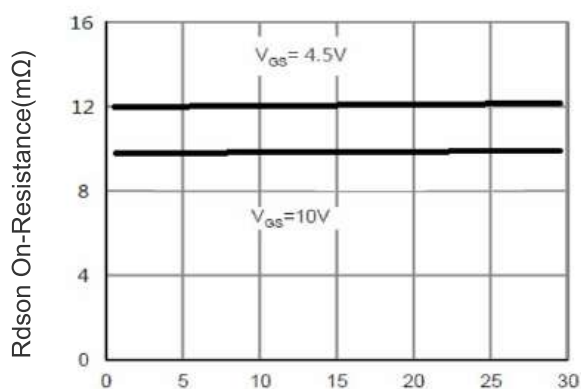
V_{GS} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



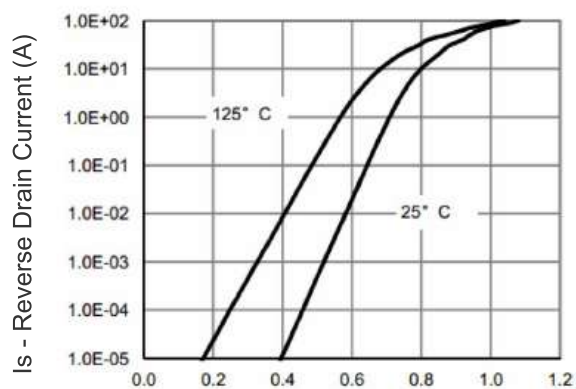
Q_g Gate Charge (nC)

Figure 5 Gate Charge



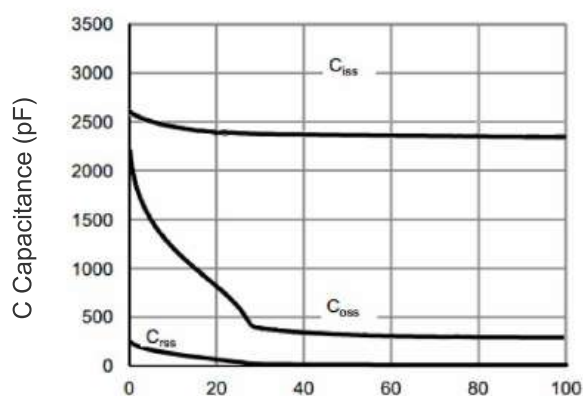
I_D - Drain Current (A)

Figure 3 $R_{DS(on)}$ - Drain Current

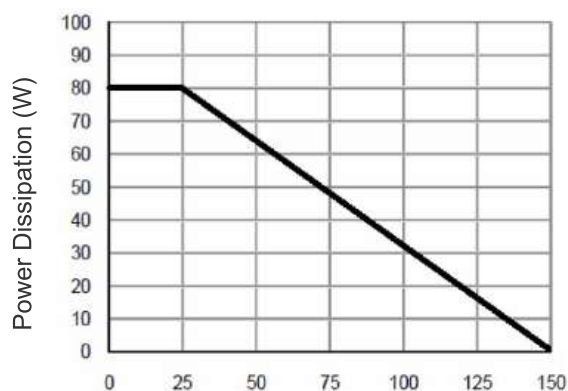


V_{SD} Source-Drain Voltage (V)

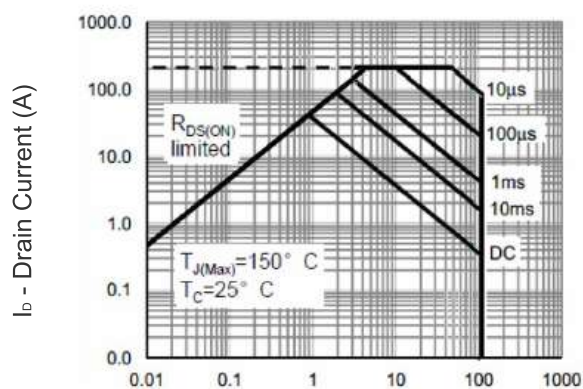
Figure 6 Source- Drain Diode Forward



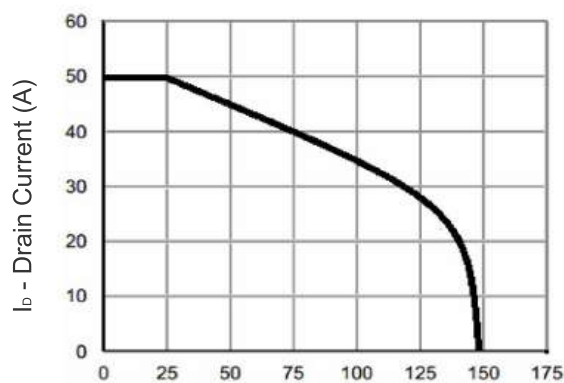
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



Tj -Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)
Figure 10 Current De-rating

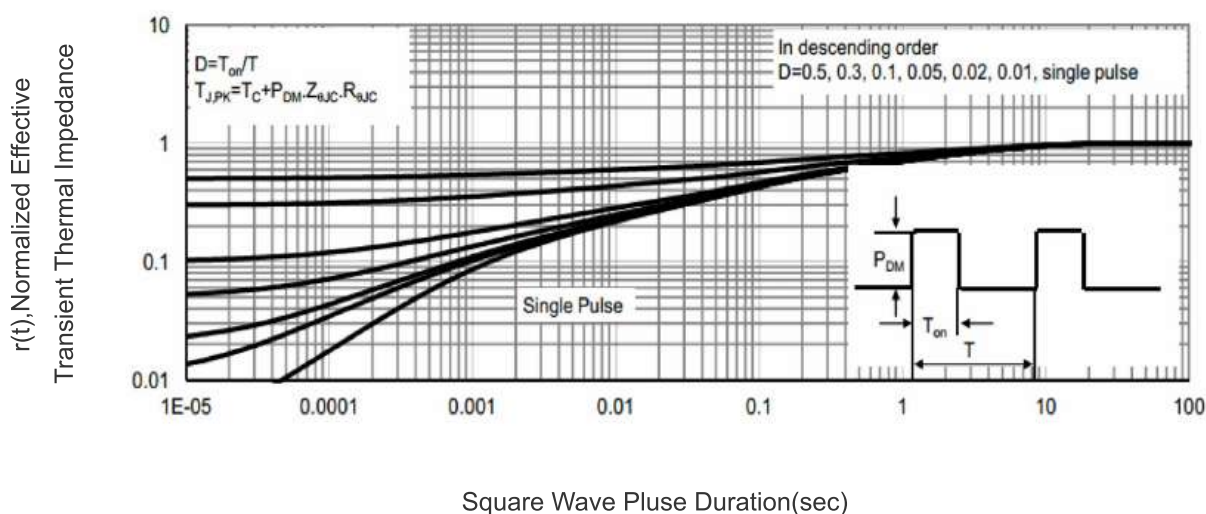
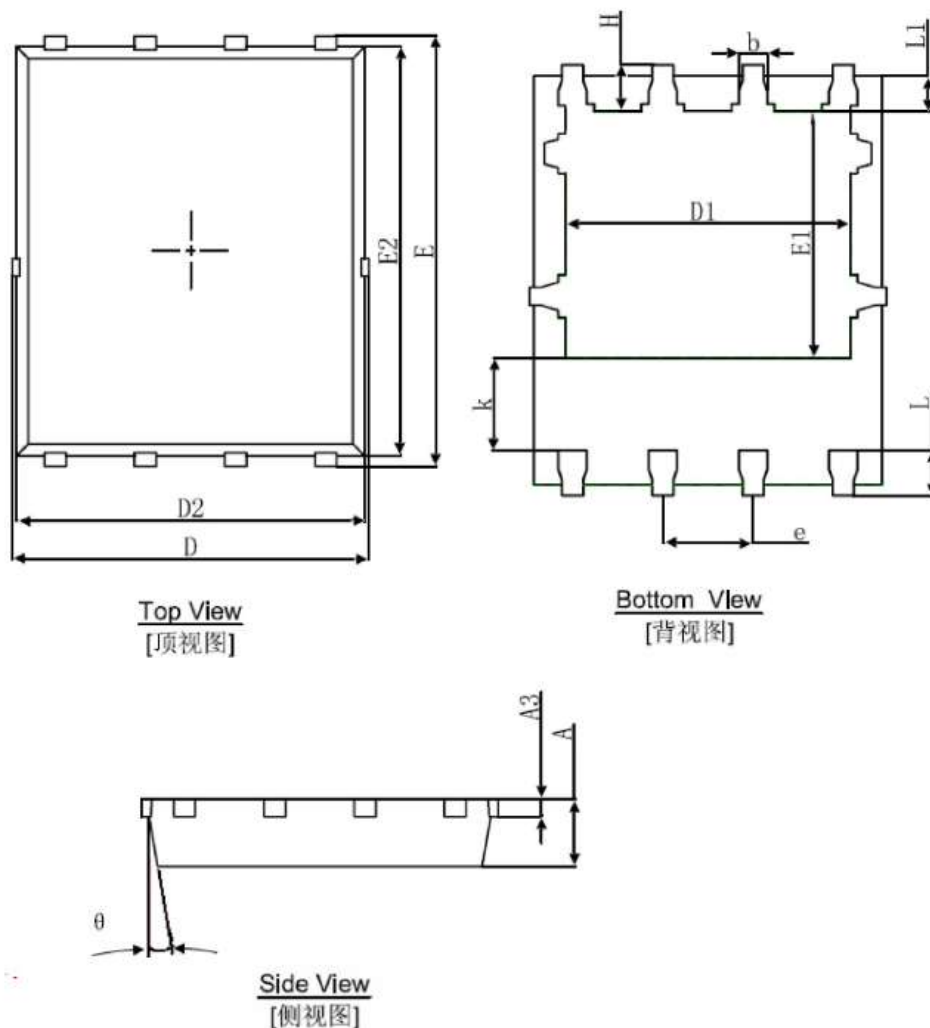


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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