

MJ N-Channel Super Trench Power MOSFET

Description

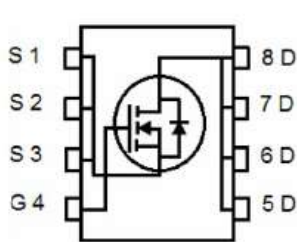
The MJXP0225G uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- ◆ $V_{DS}=200V, I_D=25A$
 $R_{DS(ON)}=33m\Omega$ (typical) @ $V_{GS}=10V$
- ◆ Excellent gate charge x $R_{DS(on)}$ product(FOM)
- ◆ Very low on-resistance $R_{DS(on)}$
- ◆ 150°C operating temperature
- ◆ Pb-free lead plating

Application

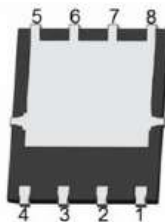
- ◆ DC/DC Converter
- ◆ Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View



Bottom View

DFN 5X6

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P0225G	MJXP0225G	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	25	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_{D(100^{\circ}C)}$	17.6	A
Pulsed Drain Current ^(Note 1)	I_{DM}	100	A
Maximum Power Dissipation	P_D	135	W
Derating factor		1.08	W/ $^{\circ}C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	320	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.93	$^{\circ}C/W$
Thermal Resistance,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	$^{\circ}C/W$

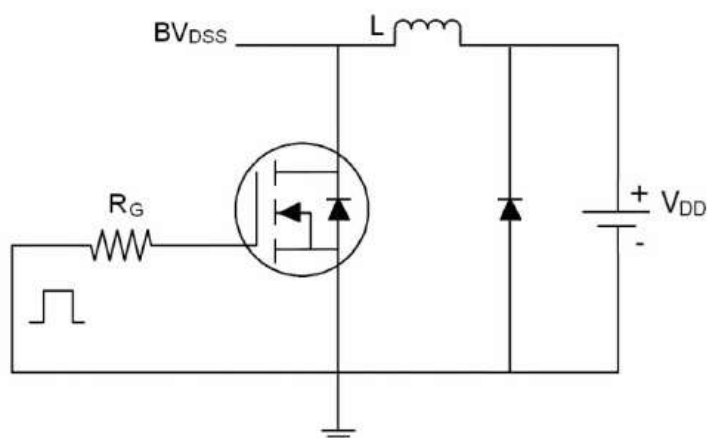
Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	200	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =200V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2.5	3.5	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V,I _D =20A	-	33	40	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =20A	15	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =100V,V _{GS} =0V F=1.0MHz	-	1660	2000	PF
Output Capacitance	C _{oss}		-	130	-	PF
Reverse Transfer Capacitance	C _{rss}		-	5.4	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =100V,R _L =7.5Ω V _{GS} =10V,R _G =3Ω	-	7	14	nS
Turn-on Rise Time	t _r		-	9	16	nS
Turn-Off Delay Time	t _{d(off)}		-	25	42	nS
Turn-Off Fall Time	t _f		-	5	9	nS
Total Gate Charge	Q _g	V _{DS} =100V,I _D =20A V _{GS} =10V	-	28	36	nC
Gate-Source Charge	Q _{gs}		-	11	14	nC
Gate-Drain Charge	Q _{gd}		-	5.9	8	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	25	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =I _S di/dt=100A/μs <small>(Note 3)</small>	-	45	-	nS
Reverse Recovery Charge	Q _{rr}		-	160	-	nC

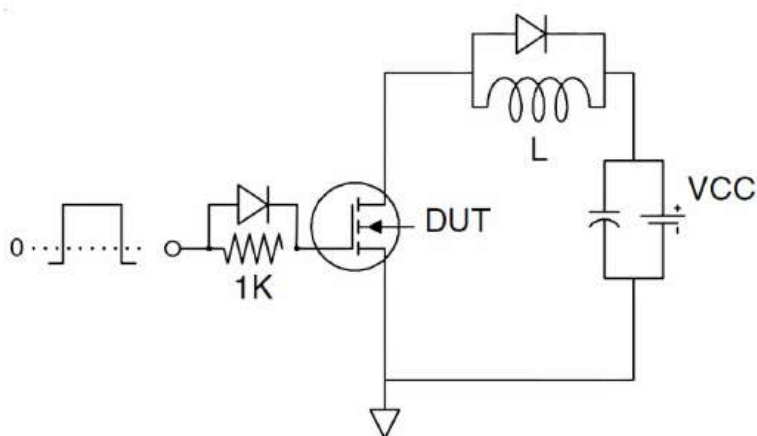
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω

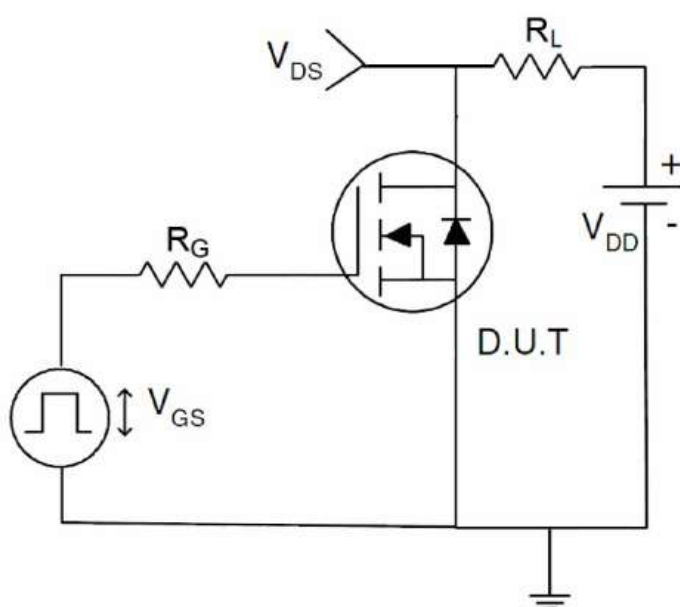
Test circuit



EAS test Circuit

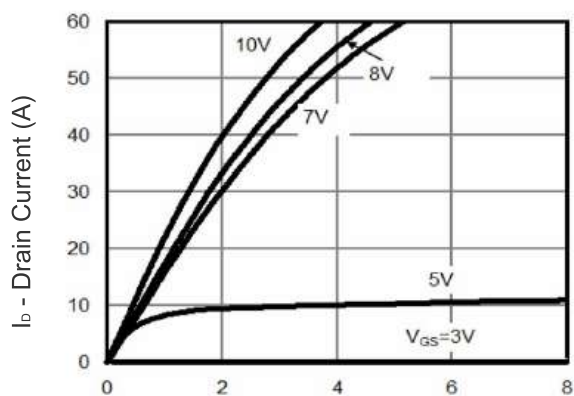


Gate charge test Circuit



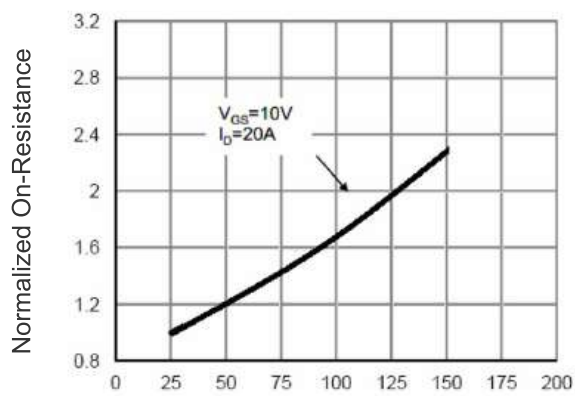
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics



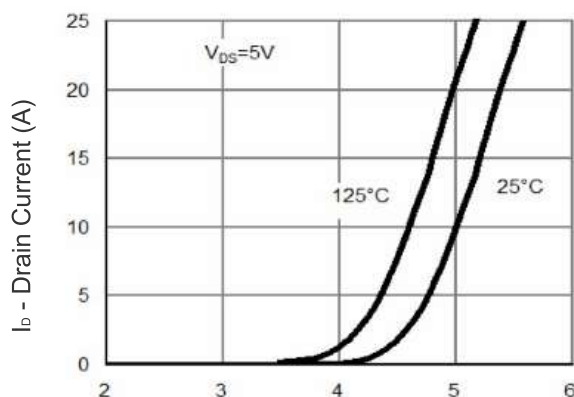
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



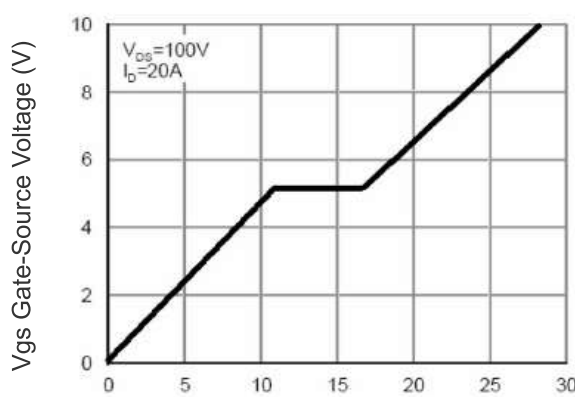
Tj -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



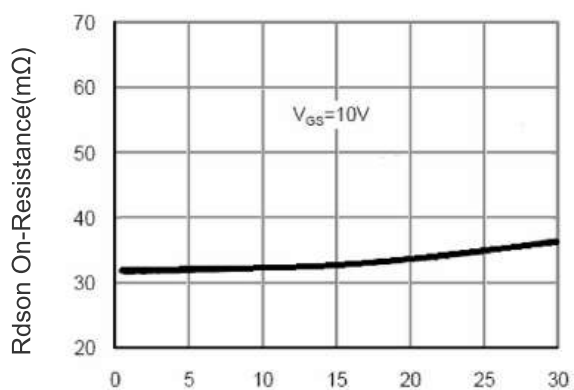
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



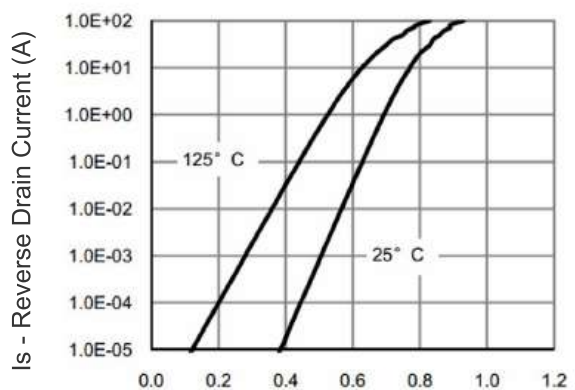
Qg Gate Charge (nC)

Figure 5 Gate Charge



Id - Drain Current (A)

Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

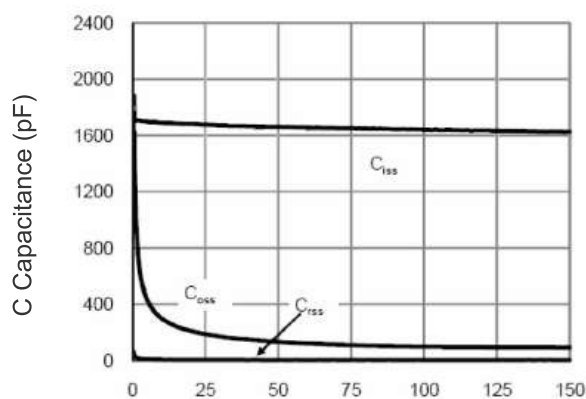


Figure 7 Capacitance vs Vds

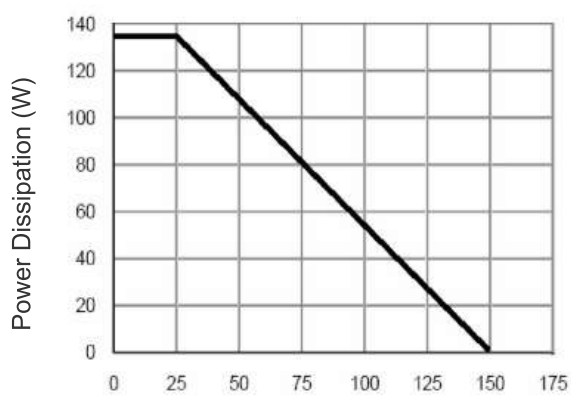


Figure 9 Power De-rating

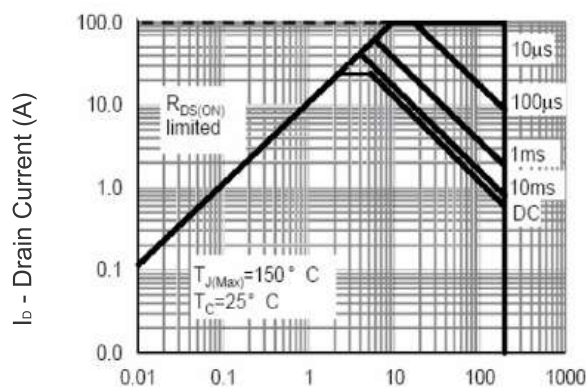


Figure 8 Safe Operation Area

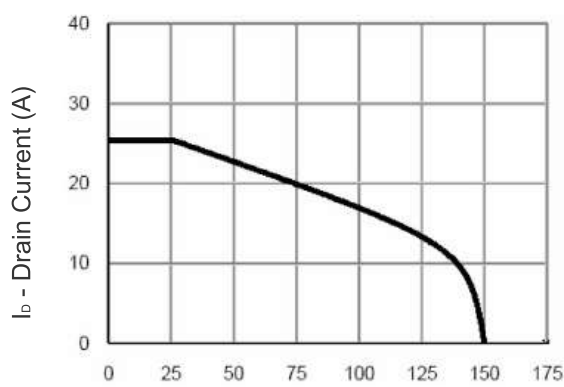


Figure 10 Current De-rating

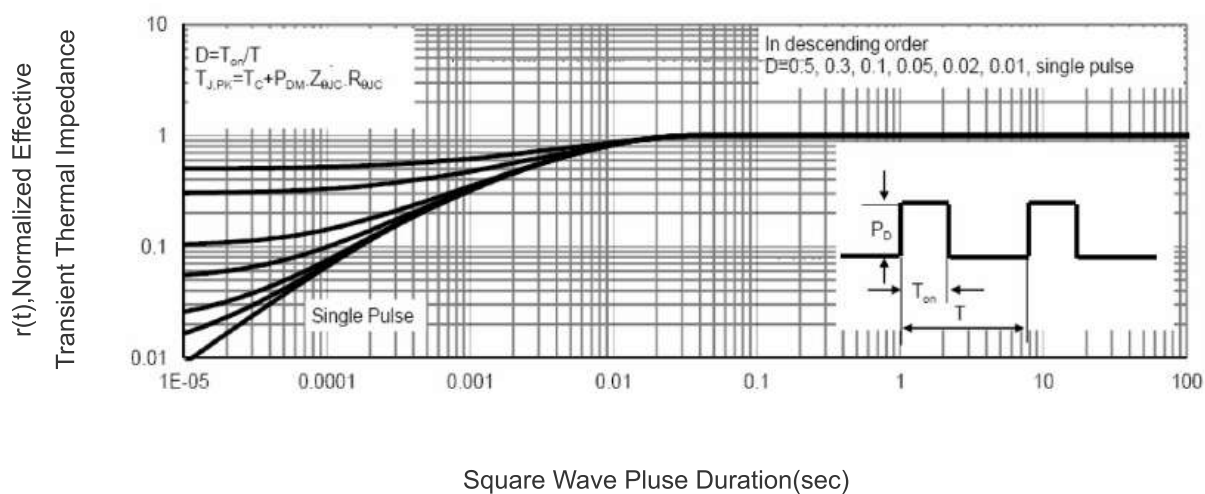
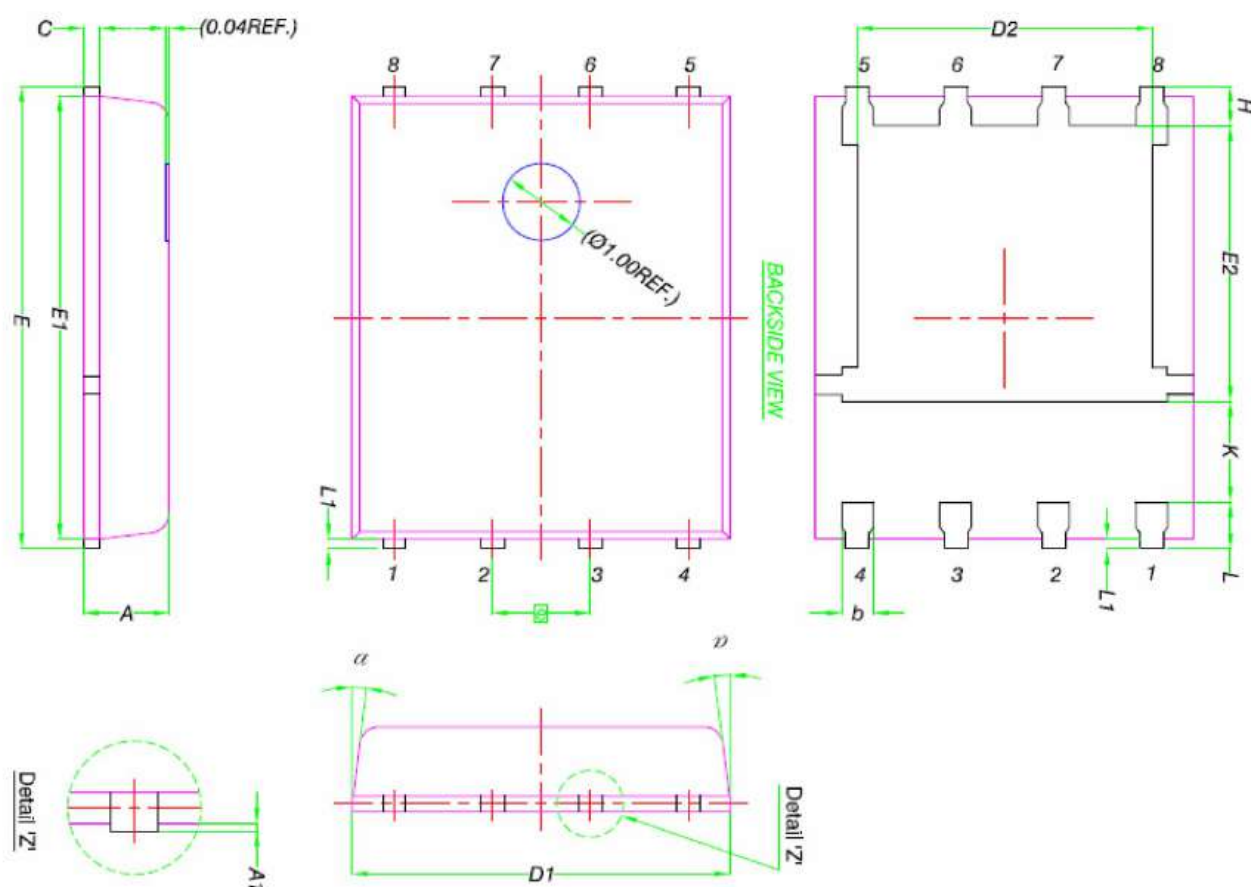
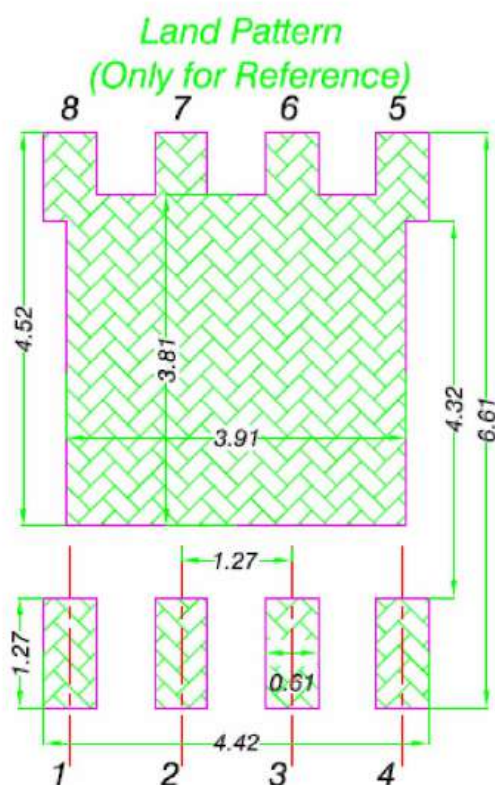


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°



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