

# MJ N-Channel Enhancement Mode Power MOSFET

## Description

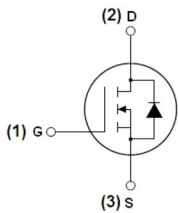
The MJ85H21T uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in automotive applications and a wide variety of other applications.

## General Features

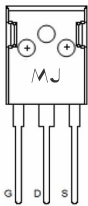
- ◆  $V_{DS}=85V, I_D=210A$   
 $R_{DS(ON)}<3.5m\Omega$  @  $V_{GS}=10V$
- ◆ Good stability and uniformity with high  $E_{AS}$
- ◆ Special process technology for high ESD capability
- ◆ High density cell design for ultra low  $R_{dson}$
- ◆ Fully characterized avalanche voltage and current
- ◆ Excellent package for good heat dissipation

## Application

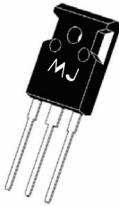
- ◆ Automotive applications
- ◆ Hard switched and high frequency circuits
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-247 top view

100% UIS TESTED! 100%  $\Delta V_{ds}$  TESTED!

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ85H21T	MJ85H21T	TO-247	-	-	-

## Absolute Maximum Ratings ( $T_c=25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	85	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	210	A
Drain Current-Continuous( $T_c=100^{\circ}\text{C}$ )	$I_{D(100^{\circ}\text{C})}$	150	A
Pulsed Drain Current	$I_{DM}$	850	A
Maximum Power Dissipation	$P_D$	330	W
Single pulse avalanche energy <sup>(Note 3)</sup>	$E_{AS}$	220	mJ
Derating factor		2.2	W/ $^{\circ}\text{C}$
Peak Diode Recovery $dv/dt$ <sup>(Note 4)</sup>	$dv/dt$	5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^{\circ}\text{C}$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 1)</sup>	$R_{\theta JA}$	0.45	$^{\circ}\text{C}/\text{W}$
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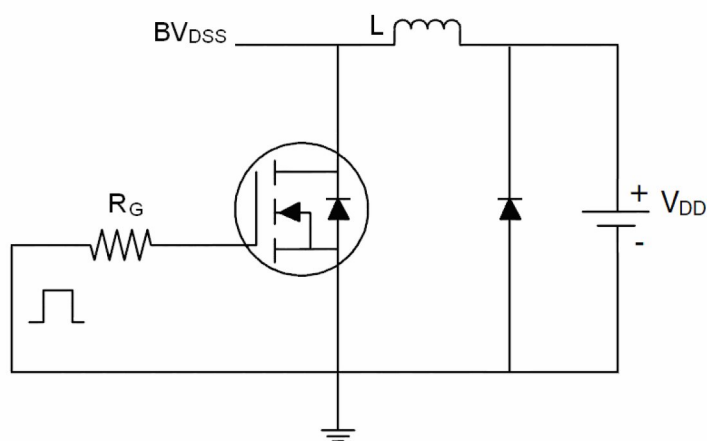
Electrical Characteristics (T<sub>A</sub> =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	85	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =85V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±200	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	2	3	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =40A	-	2.9	3.5	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V,I <sub>D</sub> =20A	35	-	-	S
Dynamic Characteristics						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V,V <sub>GS</sub> =0V, F=1.0MHz	-	11000	-	PF
Output Capacitance	C <sub>oss</sub>		-	914	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	695	-	PF
Switching Characteristics						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V,I <sub>D</sub> =2A,R <sub>L</sub> =15Ω V <sub>GS</sub> =10V,R <sub>GEN</sub> =2.5Ω	-	23	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	190	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	130	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	120	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> =30V,I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	250	-	nC
Gate-Source Charge	Q <sub>GS</sub>		-	48	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	98	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =40A	-	-	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> =25°C, I <sub>F</sub> =40A di/dt=100A/μs <sup>(Note 2)</sup>	-	63	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	98	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

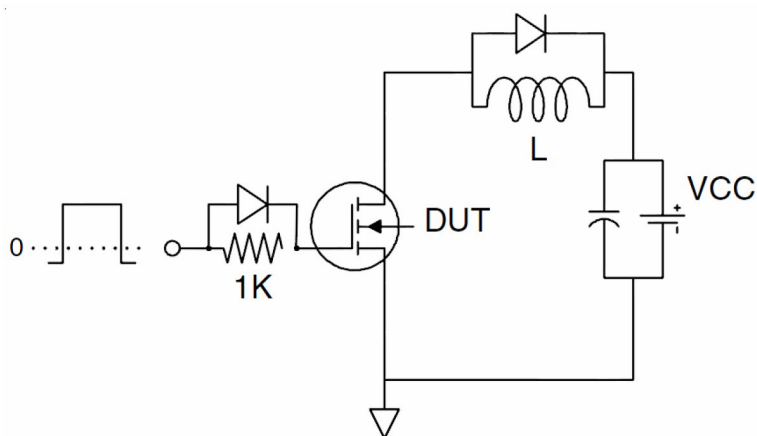
Notes:

- ① Surface Mounted on FR4 Board, t≤10sec.
- ② Pulse Test: Pulse Width≤400μs, Duty Cycle≤2%.
- ③ EAS condition：T<sub>J</sub>=25°C,V<sub>DD</sub>=42.5V,V<sub>G</sub>=10V,L=2mH,R<sub>g</sub>=25Ω,I<sub>AS</sub>=37A
- ④ I<sub>SD</sub>≤125A, di/dt≤260A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤175°C

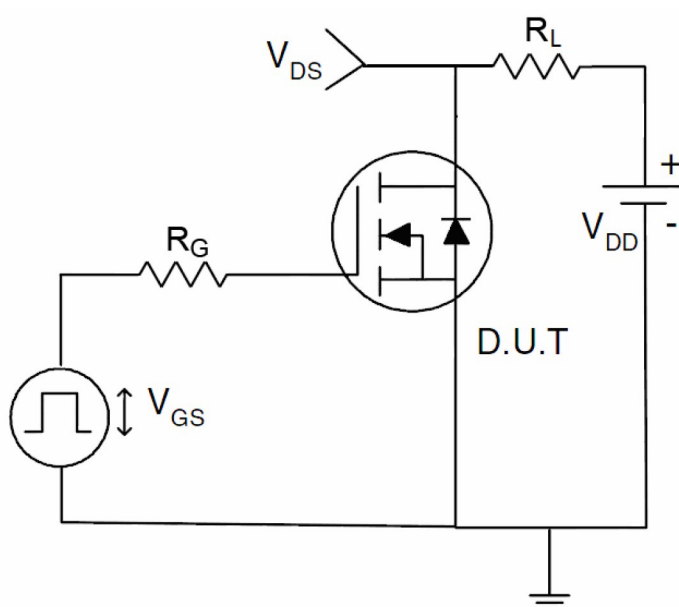
# Test circuit



EAS test Circuit

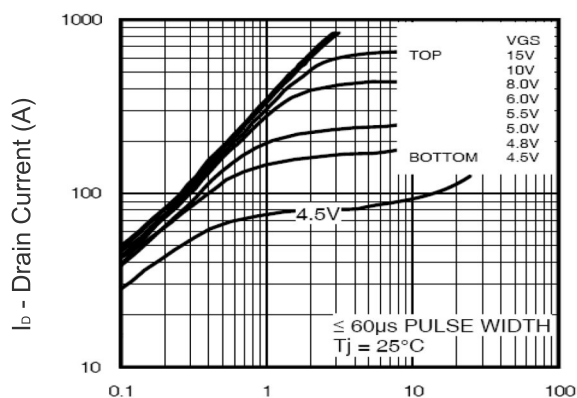


Gate charge test Circuit

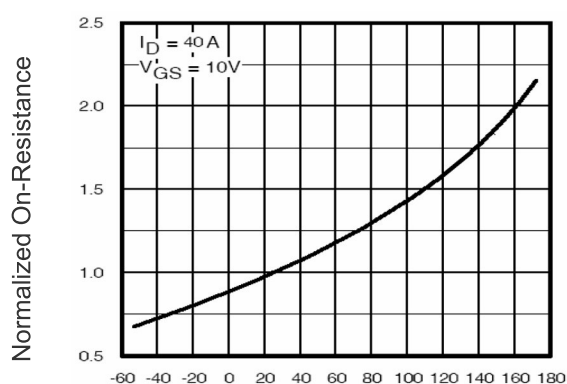


Switch Time Test Circuit

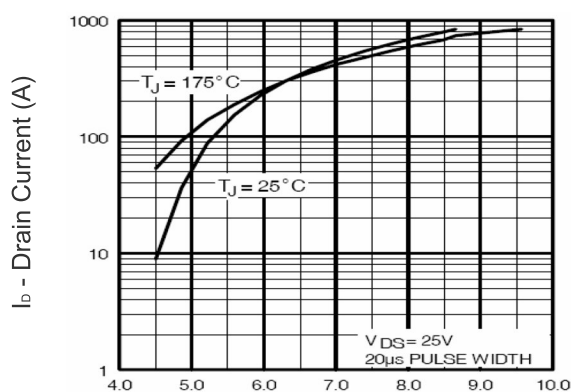
# Typical Electrical and Thermal Characteristics (Curves)



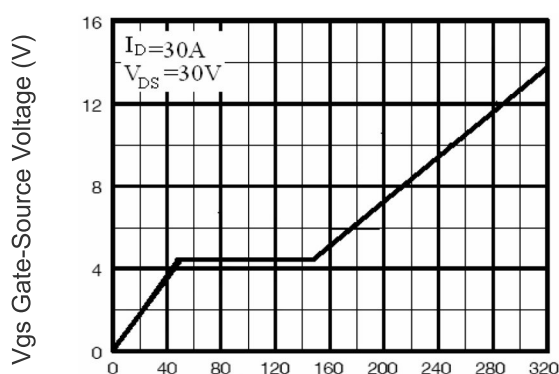
V<sub>DS</sub> Drain-Source Voltage (V)  
Figure 1 Output Characteristics



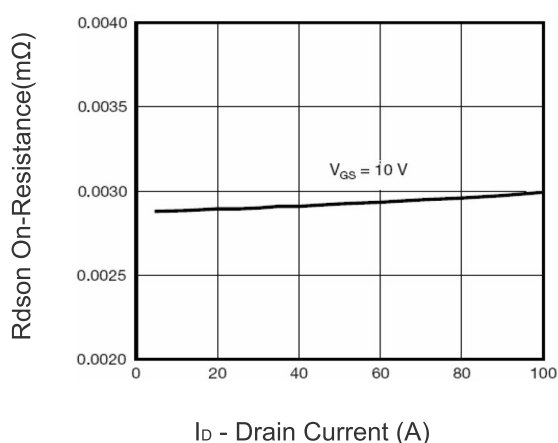
T<sub>J</sub> -Junction Temperature(°C)  
Figure 4 Rdson-Junction Temperature



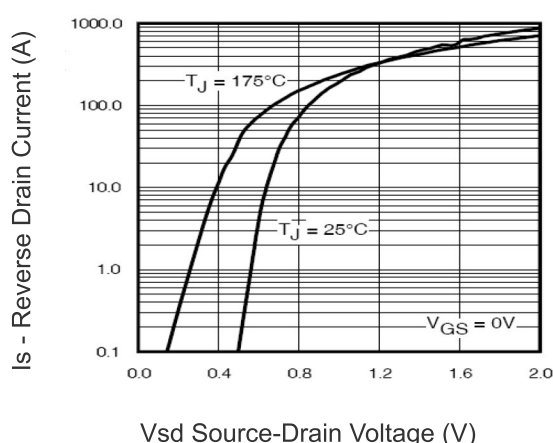
V<sub>GS</sub> Gate-Source Voltage (V)  
Figure 2 Transfer Characteristics



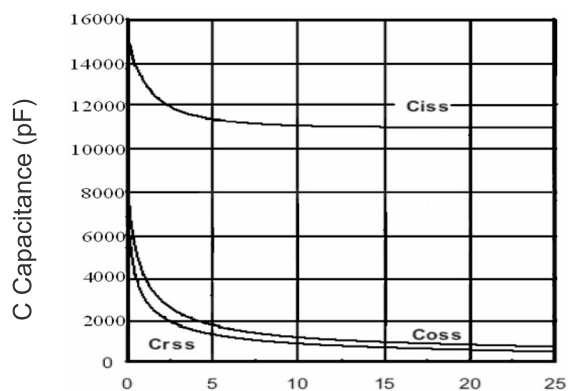
Q<sub>g</sub> Gate Charge (nC)  
Figure 5 Gate Charge



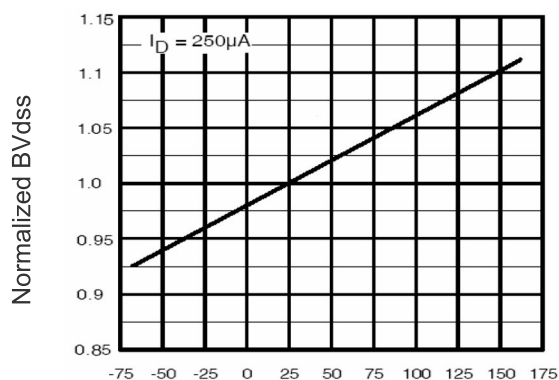
I<sub>D</sub> - Drain Current (A)  
Figure 3 Rdson- Drain Current



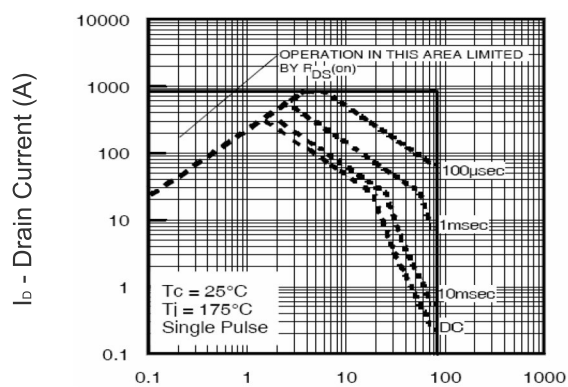
V<sub>SD</sub> Source-Drain Voltage (V)  
Figure 6 Source- Drain Diode Forward



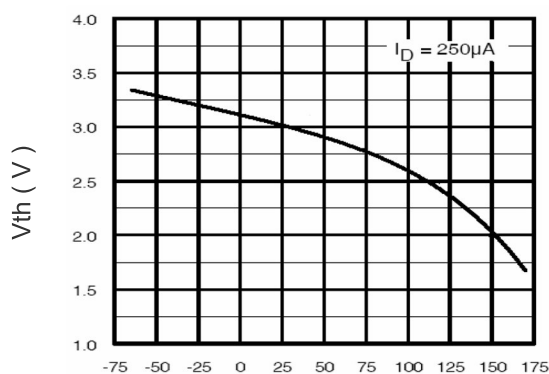
V<sub>ds</sub> Drain-Source Voltage (V)  
Figure 7 Capacitance vs V<sub>ds</sub>



T<sub>J</sub> -Junction Temperature(°C)  
Figure 9 BV<sub>DSS</sub> vs Junction Temperature



V<sub>ds</sub> Drain-Source Voltage (V)  
Figure 8 Safe Operation Area



T<sub>J</sub> -Junction Temperature(°C)  
Figure 10 V<sub>GS(th)</sub> vs Junction Temperature

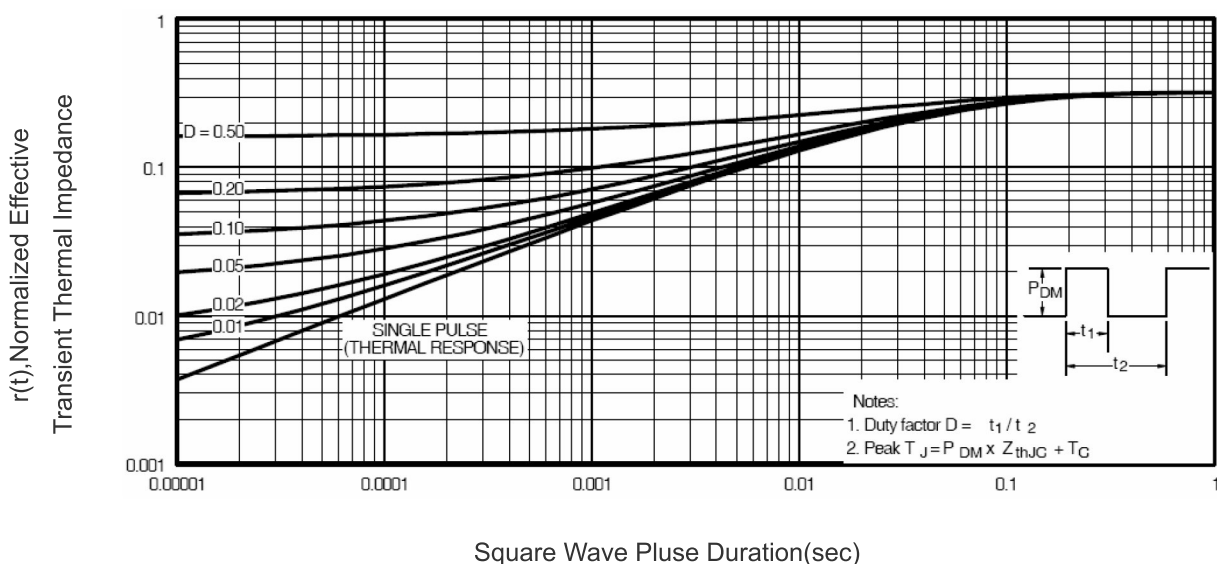
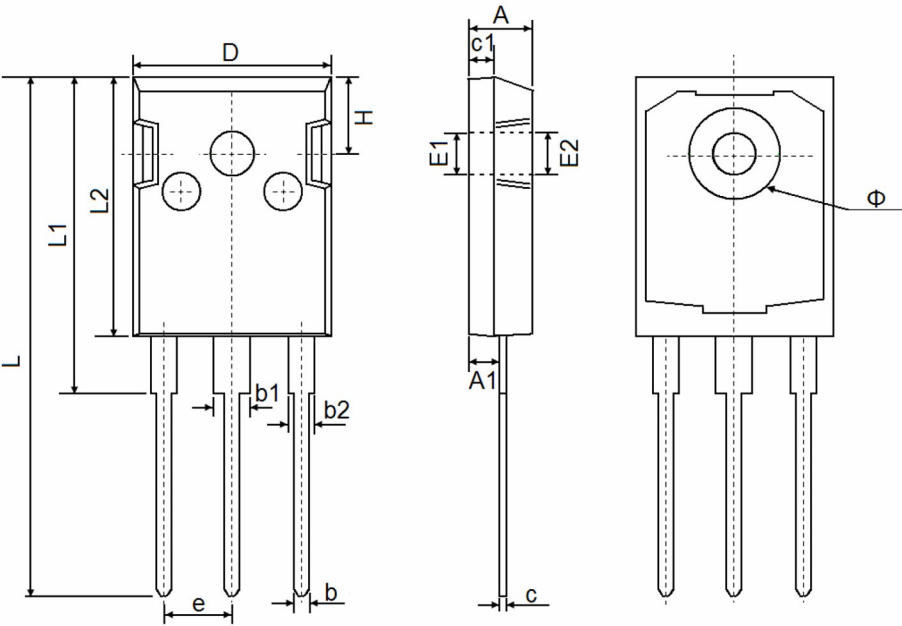


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-247 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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