



MJ N-Channel Enhancement Mode Power MOSFET

Description

The MJ82H140LL uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

General Features

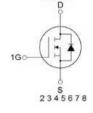
- ♦ Vps =82V.lp =140A $R_{DS(ON)} < 5.0 \text{m}\Omega$ @ $V_{GS} = 10 \text{V}$ (Typ:4.0 m Ω)
- ◆ Special process technology for high ESD capability
- ♦ High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation

Application

- ◆ Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply







TOLL

Schematic diagram

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ82H140LL	MJ82H140LL	TOLL	4	-	9

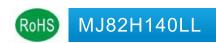
Absolute Maximum Ratings (Tc =25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	82	V
Gate-Source Voltage	Vgs	±20	V
Drain Current-Continuous	lo	140	А
Drain Current-Continuous(Tc =100℃)	ID(100°C)	99	А
Pulsed Drain Current (Note 1)	Ірм	560	А
Maximum Power Dissipation	PD	250	W
Derating factor		1.67	W/°C
Single pulse avalanche energy (Note 5)	Eas	1500	mJ
Operating Junction and Storage Temperature Range	TJ,TsTG	-55 To 175	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	Rejc	0.6	°C/W
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Electrical Characteristics (Tc =25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	<u> </u>		1	'		
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V I _D =250µA	82	-	_	V
Zero Gate Voltage Drain Current	Ipss	Vps=82V,Vgs=0V	-	-	1	μΑ
Gate-Body Leakage Current	lgss	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)	'					
Gate Threshold Voltage	VGS(th)	V _{DS} =V _{GS} ,I _D =250µA	2.0	3.0	3.8	V
Drain-Source On-State Resistance	Rds(on)	V _{GS} =10V, I _D =20A	_	4.0	5.0	mΩ
Forward Transconductance	g FS	V _{DS} =5V,I _D =20A	65	-	-	S
Dynamic Characteristics (Note 4)	1		1	-		
Input Capacitance	Clss	V _{DS} =40V,V _{GS} =0V F=1.0MHz	-	7900	_	PF
Output Capacitance	Coss		-	445	_	PF
Reverse Transfer Capacitance	Crss		-	384	-	PF
Switching Characteristics (Note 4)	'		1			
Turn-on Delay Time	t _{d(on)}		-	23	-	nS
Turn-on Rise Time	tr	VDD=30V,RL=1.5Ω	-	42	-	nS
Turn-Off Delay Time	t _{d(off)}	$V_{DD}=30V,RL=1.5\Omega$ $R_{GEN}=2.5\Omega,V_{GS}=10V$	_	75	_	nS
Turn-Off Fall Time	tf		-	26	_	nS
Total Gate Charge	Qg	V _{DS} =40V,I _D =20A V _{GS} =10V	-	158	-	nC
Gate-Source Charge	Qgs		-	32	-	nC
Gate-Drain Charge	Qgd		-	51	-	nC
Drain-Source Diode Characteristics	I	I	l	I	ı	1
Diode Forward Voltage (Note 3)	VsD	V _{GS} =0V,I _S =140A	_	_	1.2	V
Diode Forward Current (Note 2)	ls		-	-	140	А
Reverse Recovery Time	trr	TJ=25°C, IF=20A	_	50	_	nS
Reverse Recovery Charge	Qrr	di/dt=100A/µs (Note 3)	_	110	_	nC

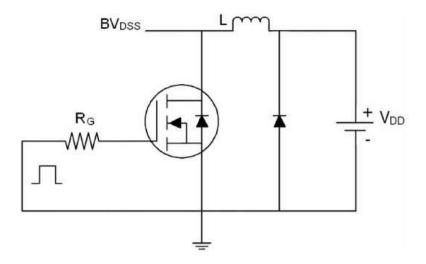
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3 Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4 Guaranteed by design, not subject to production
- (§) EAS condition: Tj=25°C,VDD=40V,VG=10V,L=0.5mH,Rg=25 Ω

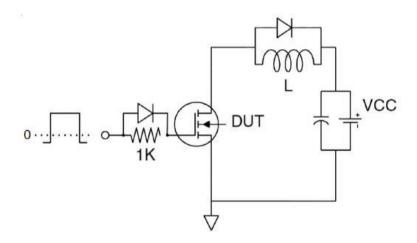




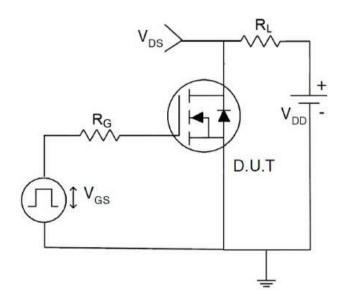
Test circuit



Eas test Circuit



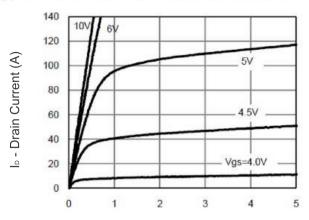
Gate charge test Circuit

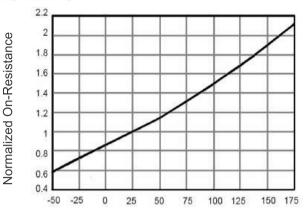


Switch Time Test Circuit



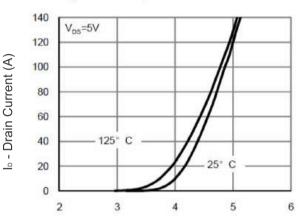
Typical Electrical and Thermal Characteristics (Curves)





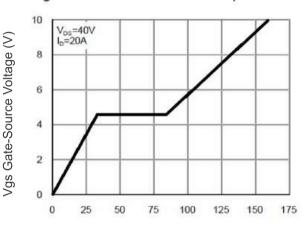
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



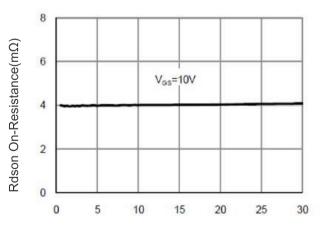
T∍ -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature

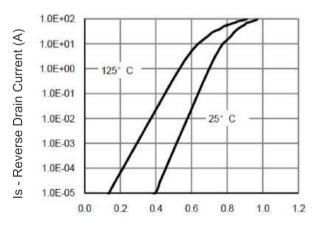


Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



Qg Gate Charge (nC)
Figure 5 Gate Charge



I⊳ - Drain Current (A)

Figure 3 Rdson- Drain Current

Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward

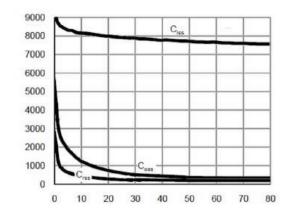


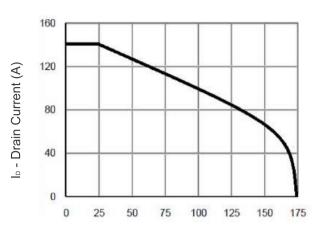
C Capacitance (pF)

lo - Drain Current (A)

r(t), Normalized Effective





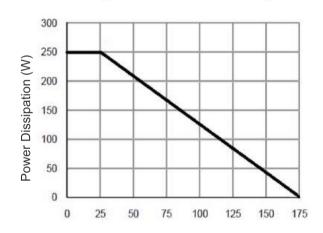


Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds

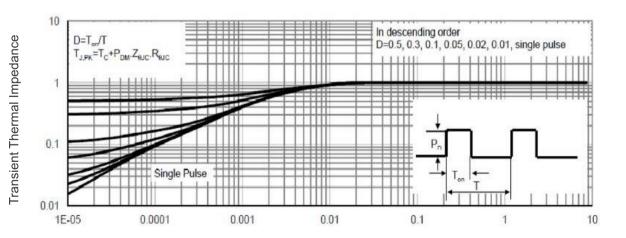
1000.0 100.0 R_{DS(ON)} limited 10.0 10ms DC 1.0 _{J(Max)}=175° 0.1 0.0 0.01 0.1 10 100 1 1000

Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area

T_J -Junction Temperature(°C)
Figure 9 Current De-rating



T_J -Junction Temperature(°C)
Figure 10 Power De-rating



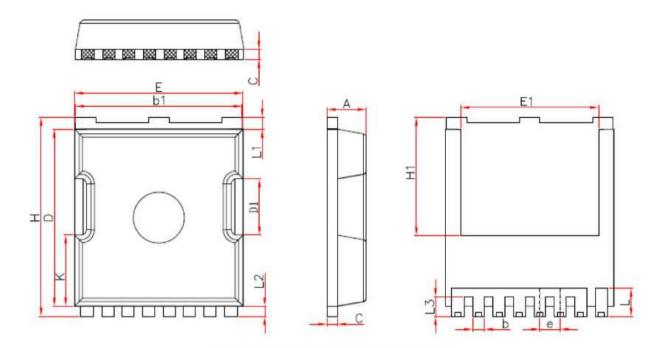
Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance





TOLL Package Information



Symbol	Millimeters			
	Min.	Nom.	Max.	
A	2.20	2.30	2.40	
b	0.65	0.75	0.85	
b1	9.70	9.80	9.90	
C	0.50	0.60	0.70	
D	10.30	10.40	10.50	
D1	3.15	3.3	3.45	
Е	9.70	9.90	10.10	
E1	8.00	8.10	8.20	
е	1.10	1.20	1.30	
Н	11.6	11.7	11.8	
H1	6.85	6.95	7.05	
K	4.08	4.18	4. 28	
L	1.60	1.65	2, 10	
L1	0.60	0.70	0.80	
L2	0.50	0.60	0.70	
L3	1.05	1.20	1.30	





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