MJ N-Channel Enhancement Mode Power MOSFET

Description

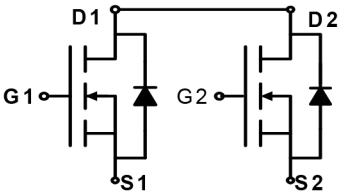
The MJ8205A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

- V_{DS} =20V,I_D =6A
  $R_{DS(ON)}$ <37mΩ @ V_{GS} =2.5V
  $R_{DS(ON)}$ <27mΩ @ V_{GS} =4.5V
- High power and current handing capability
- Lead free product is acquired
- Surface Mount Package

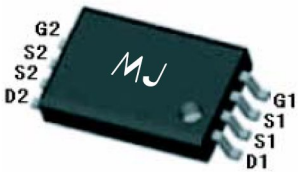
Application

- Battery protection
- Load switch
- Power management



Schematic diagram

Marking and pin Assignment



TSSOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
8205A	MJ8205A	TSSOP-8	Ø330mm	12mm	3000 units

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current-Continuous	I_D	6	A
Pulsed Drain Current (Note 1)	I_{DM}	25	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83	℃/W

Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V I_D =250μA	20	21	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =19.5V,V_{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS} =±10V,V_{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS} ,I_D =250μA	0.5	0.7	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} =4.5V, I_D =4.5A	-	21	27	mΩ
		V_{GS} =2.5V, I_D =3.5A	-	27	37	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V,I_D =4.5A	-	10	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS} =8V,V_{GS} =0V, F=1.0MHz	-	600	-	PF
Output Capacitance	C_{oss}		-	330	-	PF
Reverse Transfer Capacitance	C_{rss}		-	140	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD} =10V,I_D =1A V_{GS} =4.5V,R_{GEN} =6Ω	-	10	20	nS
Turn-on Rise Time	t_r		-	11	25	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	70	nS
Turn-Off Fall Time	t_f		-	30	60	nS
Total Gate Charge	Q_g	V_{DS} =10V,I_D =6A, V_{GS} =4.5V	-	10	15	nC
Gate-Source Charge	Q_{gs}		-	2.3	-	nC
Gate-Drain Charge	Q_{gd}		-	1.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS} =0V,I_S =1.7A	-	0.75	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	1.7	A

Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

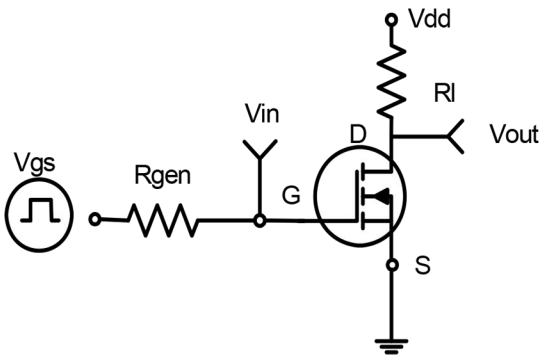


Figure 1 Switching Test Circuit

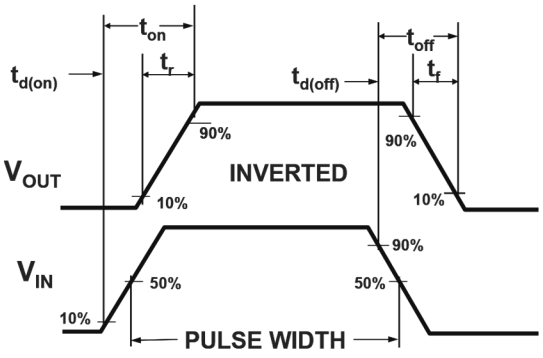


Figure 2 Switching Waveforms

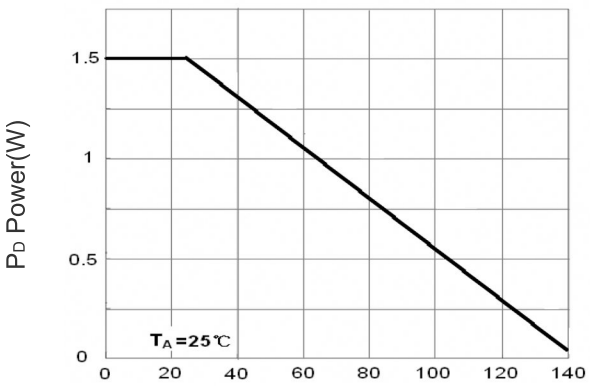


Figure 3 Power Dissipation

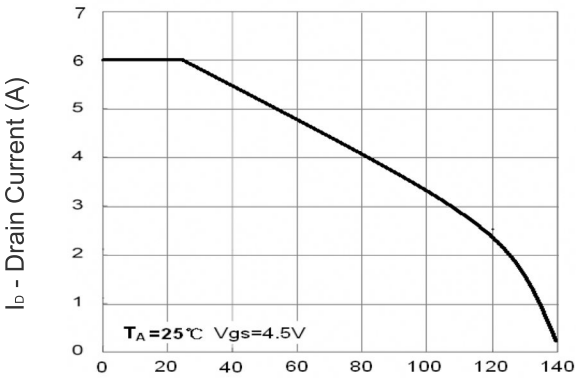


Figure 4 Drain Current

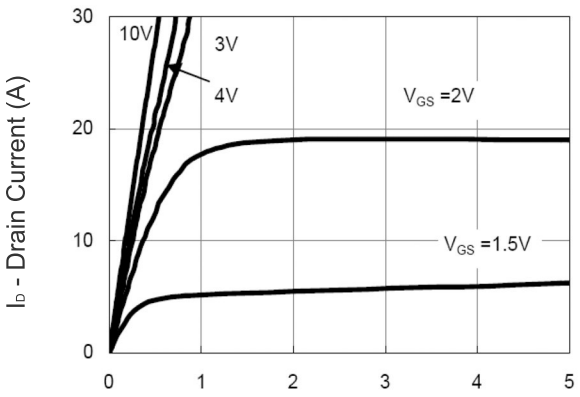


Figure 5 Output Characteristics

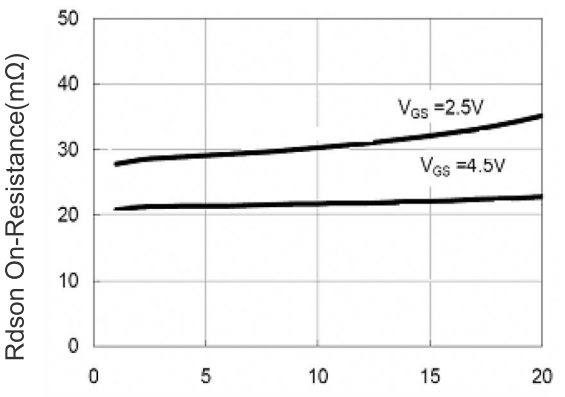


Figure 6 Drain-Source On-Resistance

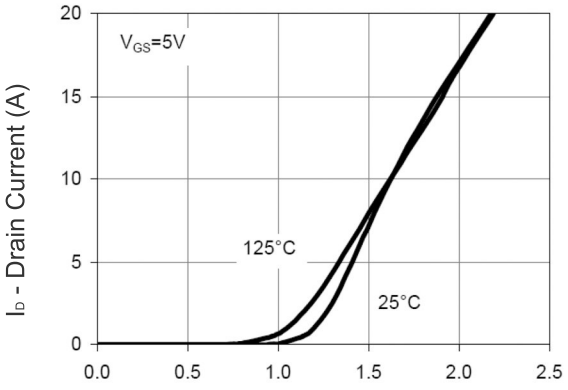


Figure 7 Transfer Characteristics

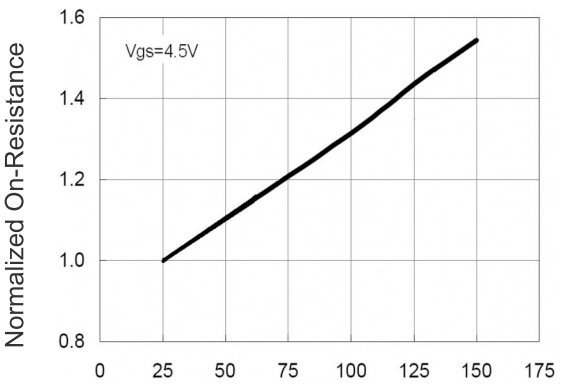


Figure 8 Drain-Source On-Resistance

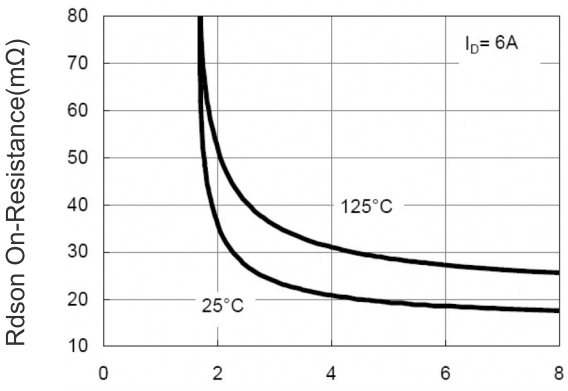


Figure 9 Rdson vs Vgs

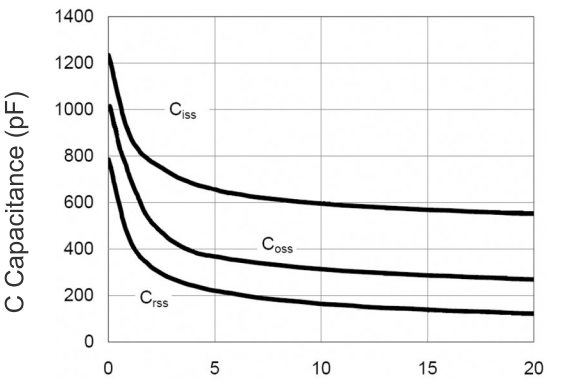


Figure 10 Capacitance vs Vds

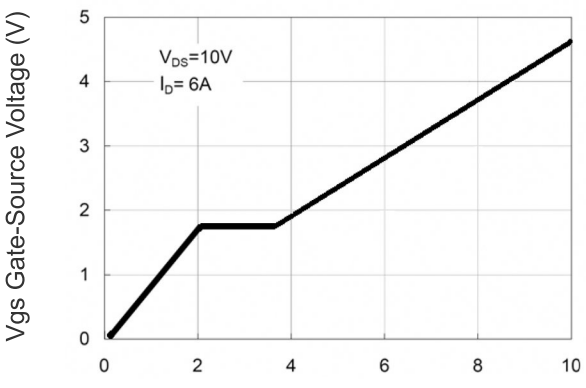


Figure 11 Gate Charge

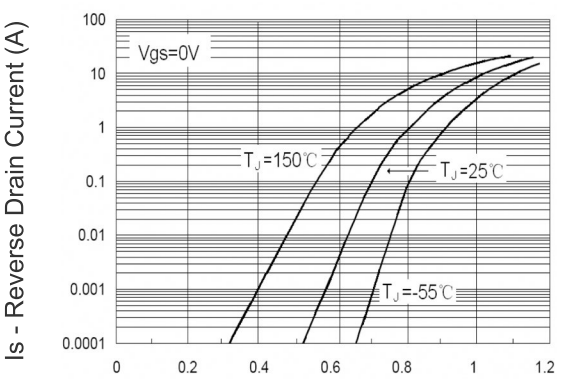


Figure 12 Source- Drain Diode Forward

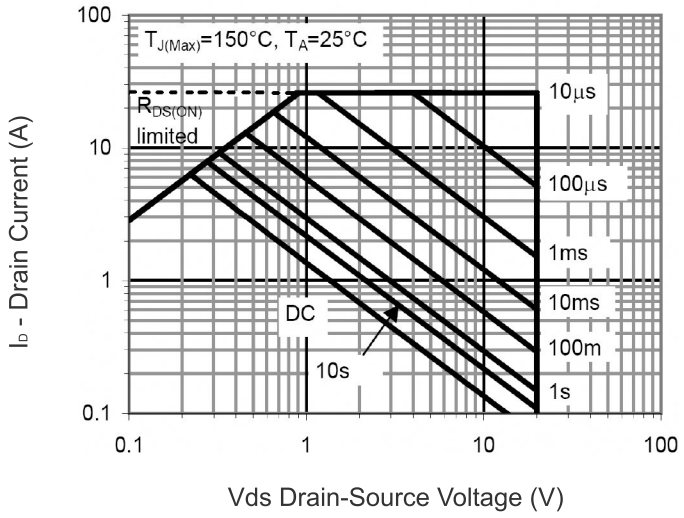


Figure 13 Safe Operation Area

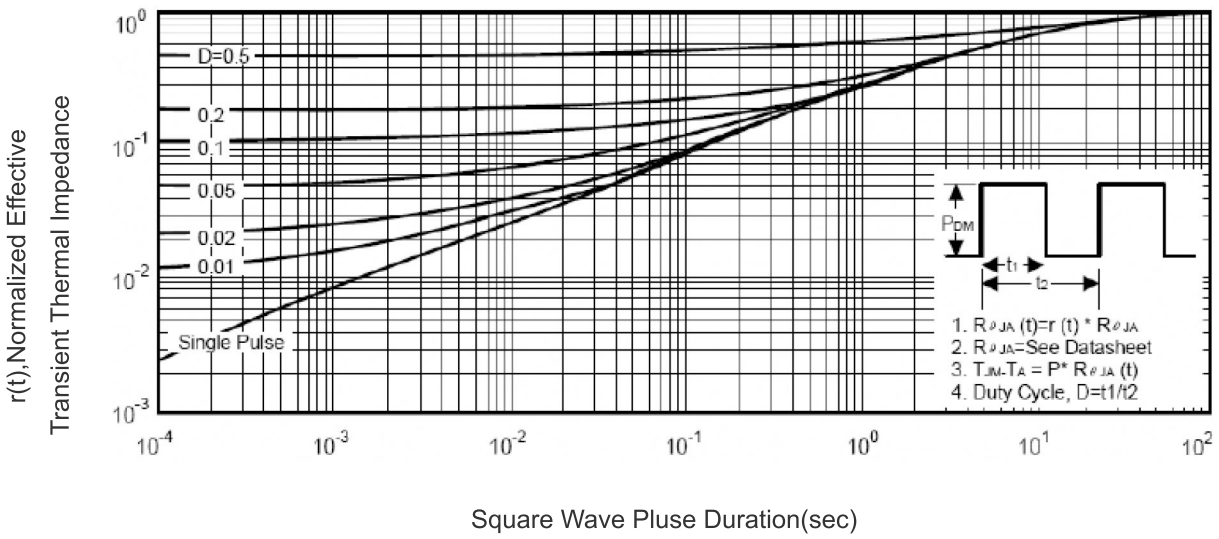
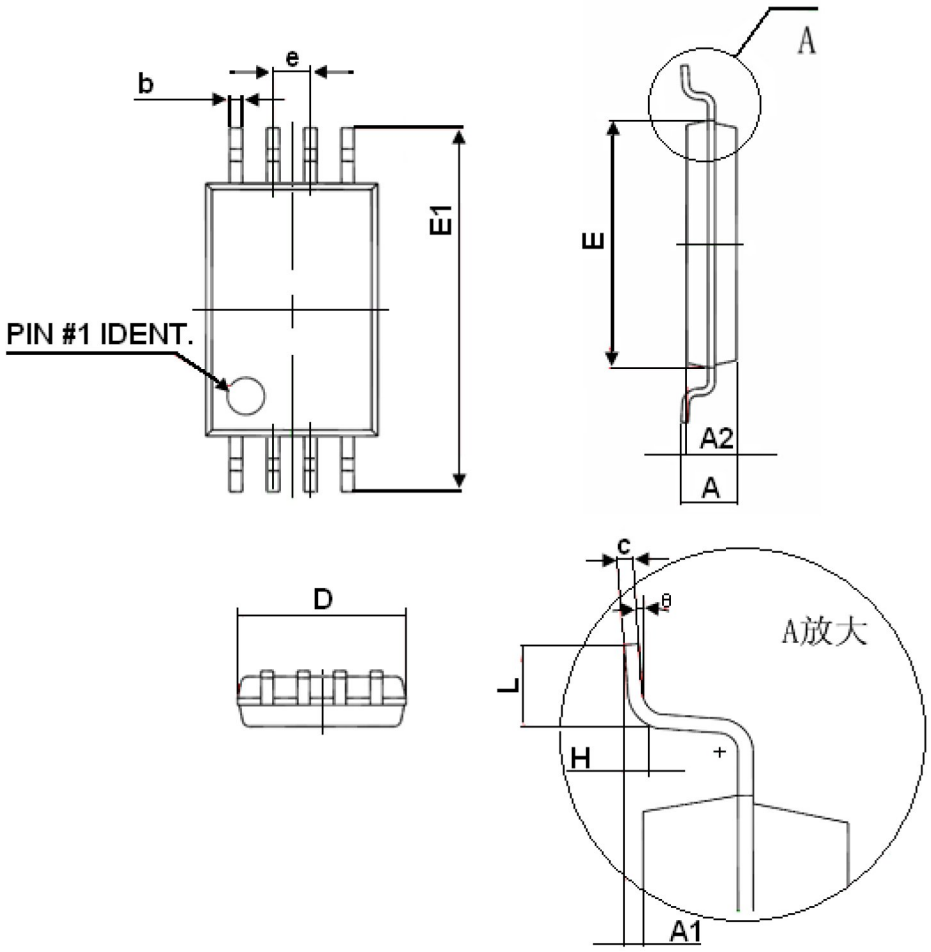


Figure 14 Normalized Maximum Transient Thermal Impedance

Tssop-8 Package Information



Symbol	Dimensions In Millimeters	
	Min	Max
D	2.900	3.100
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A		1.100
A2	0.800	1.000
A1	0.020	0.150
e	0.65(BSC)	
L	0.500	0.700
H	0.25(TYP)	
Θ	1°	7°

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