MJ N-Channel Enhancement Mode Power MOSFET

Description

The MJ7560K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

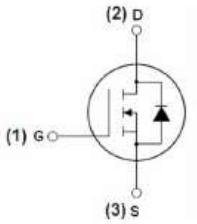
- V_{DS} =75V,I_D =60A @ V_{GS}=10V
  $R_{DS(ON)}$ <8.5mΩ @ V_{GS}=10V
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

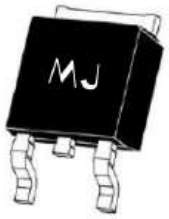
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Product Summary

BV_{DSS}	typ	84	V
$R_{DS(ON)}$	typ	6.8	mΩ
	max	8.5	mΩ
I_D		60	A



Schematic diagram



TO-252-2L top view

100% UIS TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ7560K	MJ7560K	TO-252-2L	-	-	-

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	75	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±20	V
Drain Current (DC) at Tc=25℃	$I_{D\ (DC)}$	60	A
Drain Current (DC) at Tc=100℃	$I_{D\ (DC)}$	42	A
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_{DM\ (pluse)}$	310	A
Peak diode recovery voltage	dv/dt	30	V/ns
Maximum Power Dissipation(Tc=25℃)	P_D	140	W
Derating factor		0.95	W/℃
Single pulse avalanche energy (Note 2)	E_{AS}	300	mJ
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 175	℃

Table 2. Thermal Characteristic

Thermal Resistance,Junction-to-Case (Maximum)	R_{thJC}	1.05	℃/W
Thermal Resistance,Junction-to-Ambient (Maximum)	R_{thJA}	50	℃/W

Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature

② EAS condition: Tj=25℃,V_{DD}=37.5V,V_G=10V,L=0.5mH

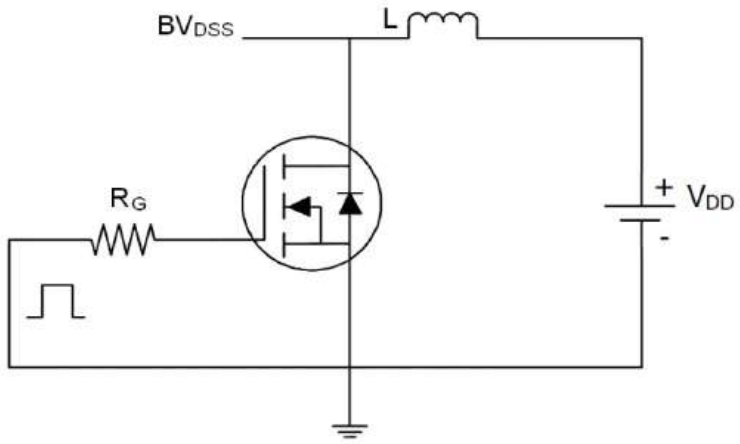
Table 3. Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	75	84	-	V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=75V,V_{GS}=0V	-	-	1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=75V,V_{GS}=0V	-	-	10	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	6.8	8.5	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=30A	-	66	-	S
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V F=1.0MHz	-	4400	-	PF
Output Capacitance	C_{oss}		-	340	-	PF
Reverse Transfer Capacitance	C_{rss}		-	260	-	PF
Total Gate Charge	Q_g	V_{DS}=30V,I_D=30A V_{GS}=10V	-	100	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	nC
Gate-Drain Charge	Q_{gd}		-	30	-	nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	17.8	-	nS
Turn-on Rise Time	t_r		-	11.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	56	-	nS
Turn-Off Fall Time	t_f		-	14.6	-	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}		-	-	80	A
Pulsed Source-drain current(Body Diode)	I_{SDM}		-	-	320	A
Forward on voltage (Note 1)	V_{SD}	T_j=25℃,I_{SD}=30A,V_{GS}=0V	-	-	1.2	V
Reverse Recovery Time (Note 1)	t_{rr}	T_J=25°C, I_F=75A di/dt=100A/μs	-	-	36	nS
Reverse Recovery Charge (Note 1)	Q_{rr}		-	-	56	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by L_S+L_D)				

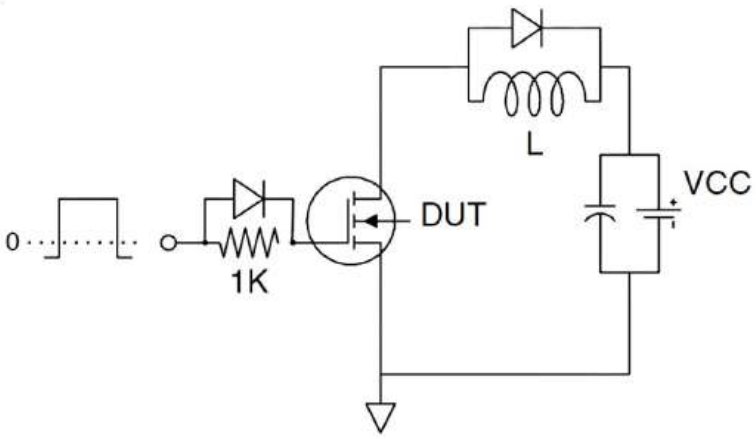
Notes:

① Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 1.5%, R_G=25Ω, Starting Tj=25℃

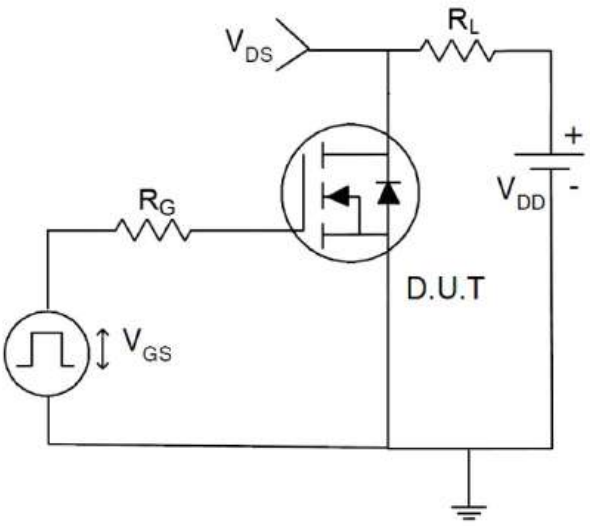
Test circuit



EAS test Circuit



Gate charge test Circuit



Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)

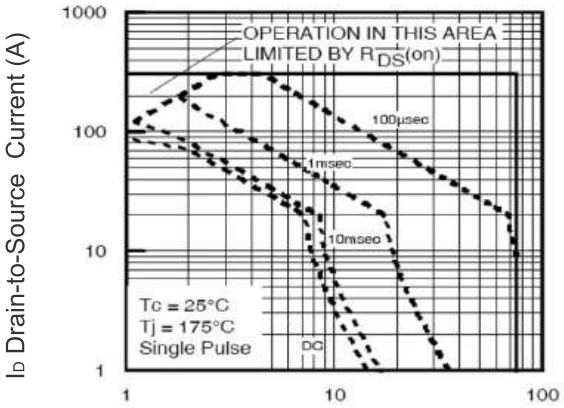


Figure 1 Safe operating area

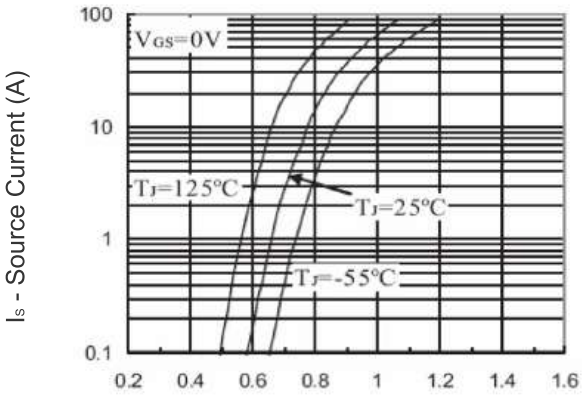


Figure 2 Source-Drain Diode Forward Voltage

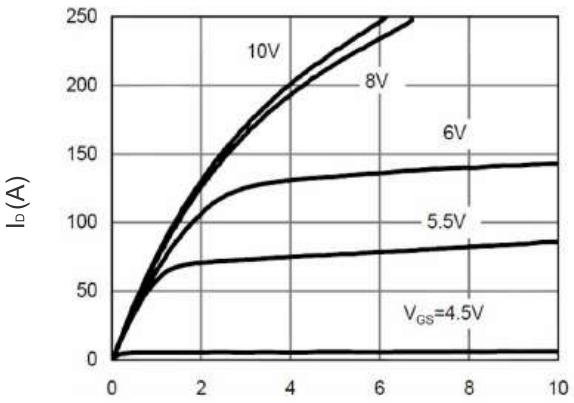


Figure 3 Output characteristics

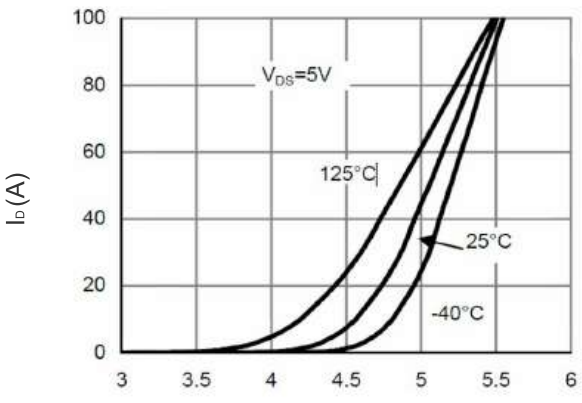


Figure 4 Transfer characteristics

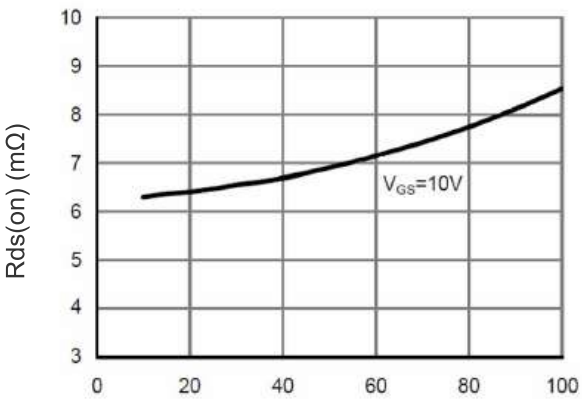


Figure 5 Static drain-source on resistance

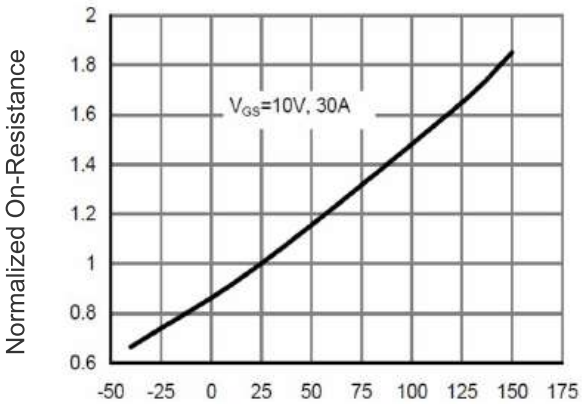


Figure 6 RDS(ON) vs Junction Temperature

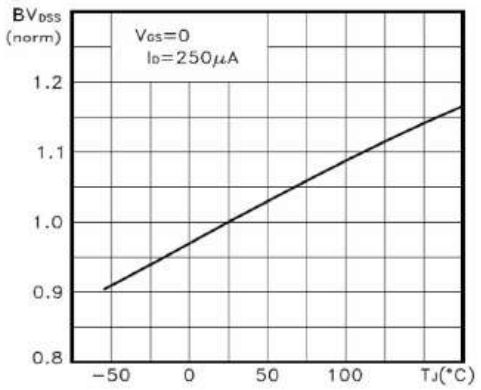


Figure 7 BV_{DSS} vs Junction Temperature

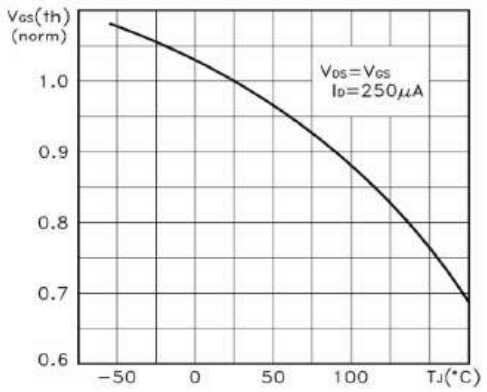


Figure 8 $V_{GS(th)}$ vs Junction Temperature

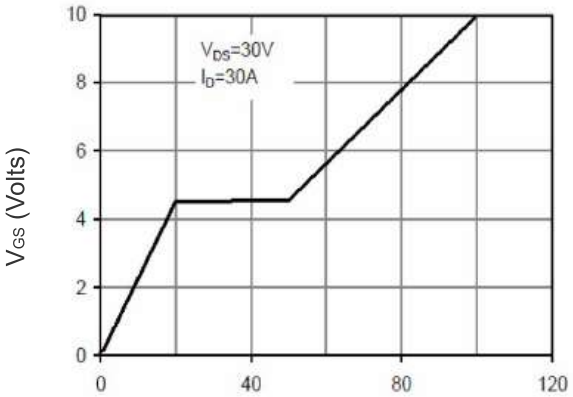


Figure 9 Gate charge waveforms

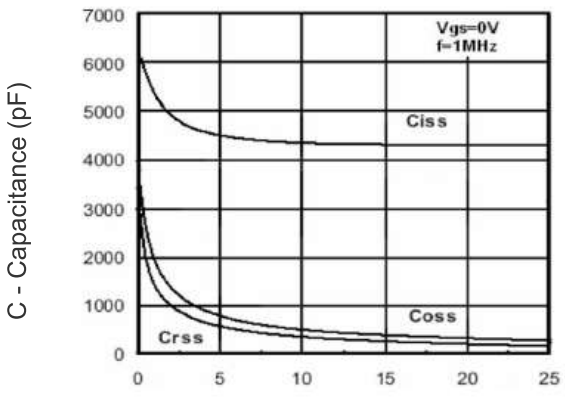


Figure 10 Capacitance

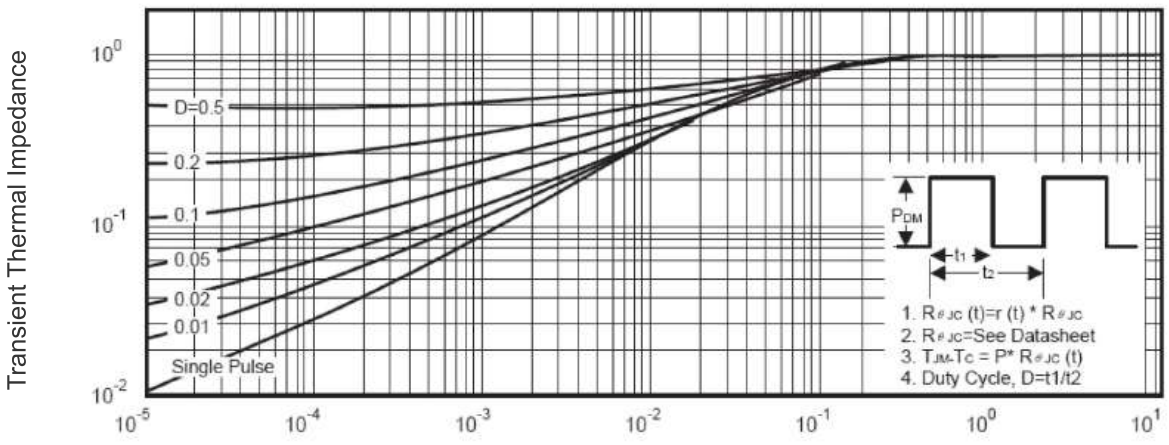
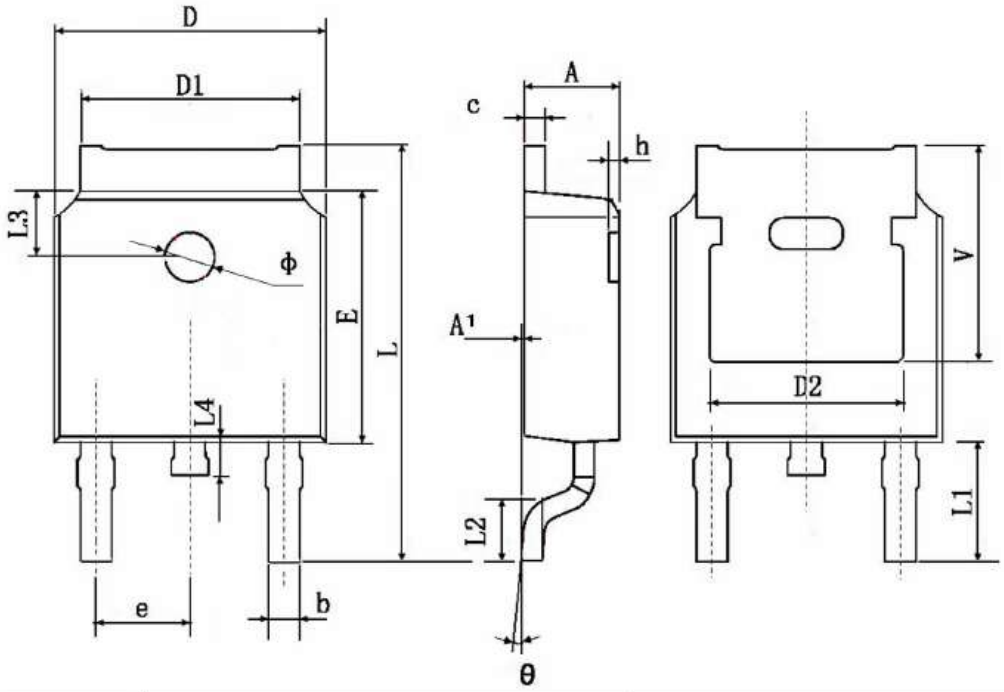


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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