N-Channel Super Junction Power MOSFET Ⅱ

General Description

The series of devices use advanced super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

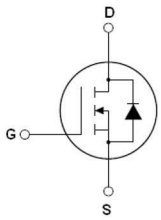
Features

- ◆ New technology for high voltage device
- ◆ Low on-resistance and low conduction losses
- ◆ Small package
- ◆ Ultra Low Gate Charge cause lower driving requirements
- ◆ 100% Avalanche Tested
- ◆ ROHS compliant

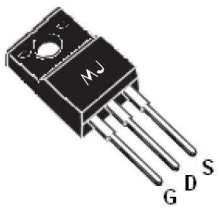
Application

- ◆ Power factor correction（PFC）
- ◆ Switched mode power supplies(SMPS)
- ◆ Uninterruptible Power Supply（UPS）

V_{DS}	700	V
$R_{DS(ON)TYP.}$	1200	mΩ
I_D	4	A



Schematic diagram



TO-220F

Package Marking And Ordering Information

Device	Device Package	Marking
MJ70R1K2F	TO-220F	MJ70R1K2F

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	MJ70R1K2F	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	700	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±30	V
Continuous Drain Current at Tc=25°C	I_D (DC)	4*	A
Continuous Drain Current at Tc=100°C	I_D (DC)	2.5	A
Pulsed drain current (Note 1)	I_{DM} (pluse)	12	A
Maximum Power Dissipation (Tc=25℃)	P_D	28.5	W
Derate above 25°C	P_D	0.23	W/°C
Single pulse avalanche energy (Note 2)	E_{AS}	130	mJ
Avalanche current (Note 1)	I_{AR}	2	A
Repetitive Avalanche energy, t_{AR} limited by T_{jmax} (Note 1)	E_{AR}	0.2	mJ

Parameter	Symbol	MJ70R1K2F	Unit
Drain Source voltage slope, V_{DS} ≤480 V	dv/dt	50	V/ns
Reverse diode dv/dt, V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+150	°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	MJ70R1K2F	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	4.4	°C/W
Thermal Resistance，Junction-to-Ambient（Maximum）	R_{thJA}	80	°C/W

Table 3. Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	700	-	-	V
Zero Gate Voltage Drain Current (Tc=25℃)	I_{DSS}	V_{DS}=700V,V_{GS}=0V	-	-	1	μA
Zero Gate Voltage Drain Current (Tc=125℃)	I_{DSS}	V_{DS}=700V,V_{GS}=0V	-	-	50	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3	3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=2.5A	-	1200	1400	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS}=20V,I_D=2.5A	-	4	-	S
Input Capacitance	C_{ies}	V_{DS}=50V,V_{GS}=0V F=1.0MHz	-	280	-	PF
Output Capacitance	C_{oss}		-	26	-	PF
Reverse Transfer Capacitance	C_{rss}		-	2.3	-	PF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=4A V_{GS}=10V	-	6.5	10	nC
Gate-Source Charge	Q_{gs}		-	1.3	-	nC
Gate-Drain Charge	Q_{gd}		-	2.5	-	nC
Intrinsic gate resistance	R_G	f=1 MHz open drain	-	2.5	-	Ω
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=380V,I_D=2.5A R_G=20Ω,V_{GS}=10V	-	6	-	nS
Turn-on Rise Time	t_r		-	3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	48	60	nS
Turn-Off Fall Time	t_f		-	8	15	nS
Source- Drain Diode Characteristics						
Source-drain current (Body Diode)	I_{SD}	T_C=25°C	-	-	4	A
Pulsed Source-drain current (Body Diode)	I_{SDM}		-	-	12	A
Forward On Voltage	V_{SD}	T_j=25°C,I_{SD}=4A,V_{GS}=0V	-	1	1.3	V
Reverse Recovery Time	t_{rr}	T_j=25°C,I_F=4A di/dt=100A/μs	-	150	-	nS
Reverse Recovery Charge	Q_{rr}		-	0.85	-	uC
Peak reverse recovery current	I_{rrm}		-	11	-	A

Notes

1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.T_j=25℃,V_{DD}=50V,V_G=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

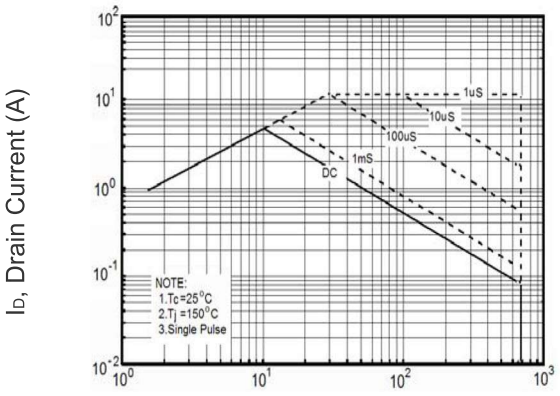


Figure 1 Safe operating area

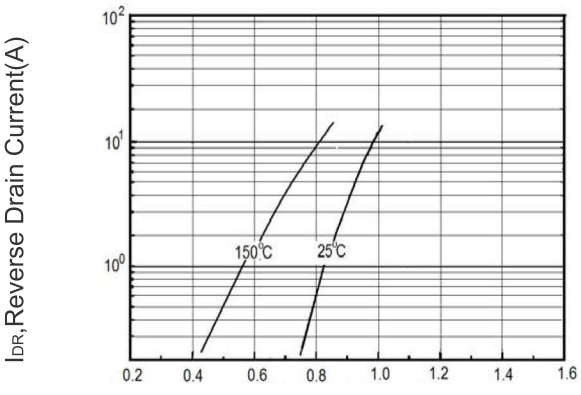


Figure 2 Source-Drain Diode Forward Voltage

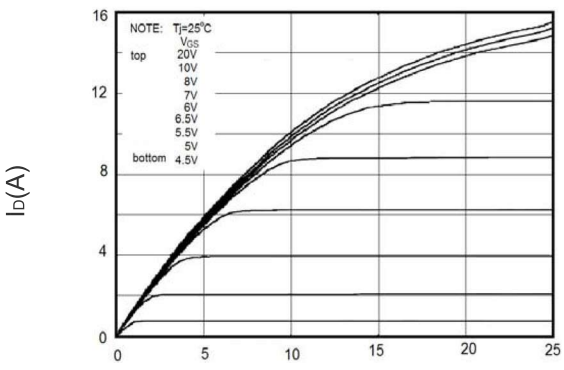


Figure 3 Output characteristics

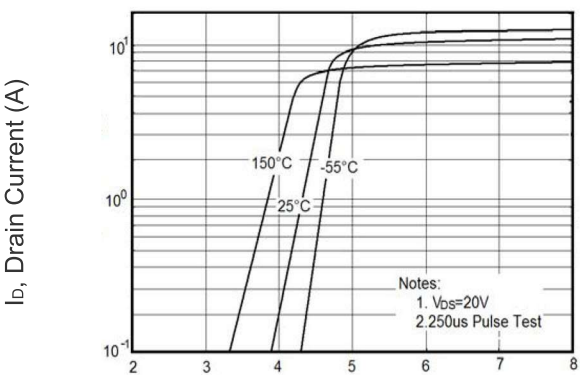


Figure 4 Transfer characteristics

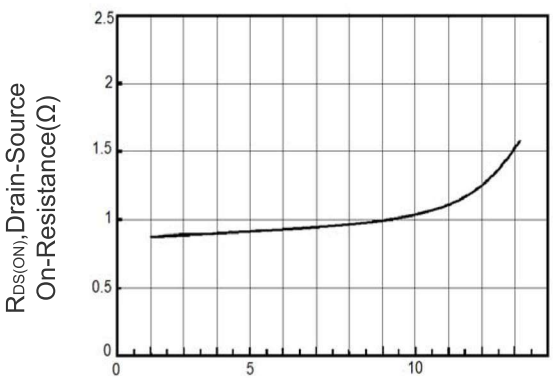


Figure 5 Static drain-source on resistance

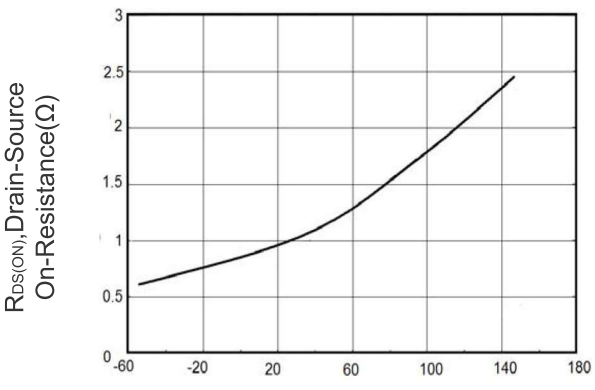


Figure 6 $R_{DS(ON)}$ vs Junction Temperature

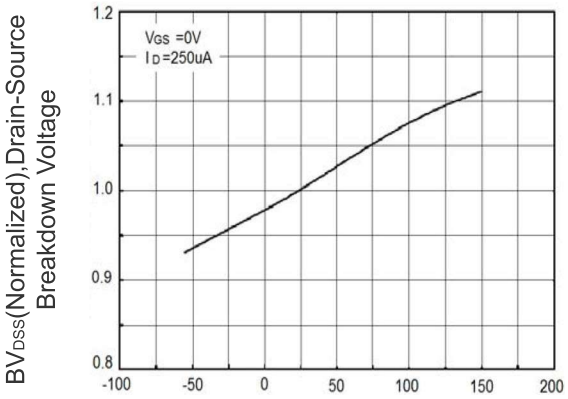


Figure 7 BV_{DSS} vs Junction Temperature

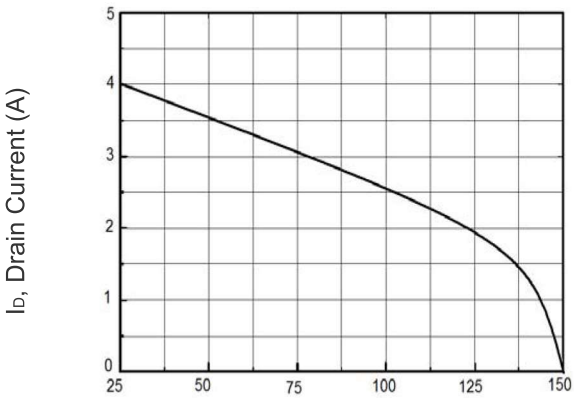


Figure 8 Maximum I_D vs Junction Temperature

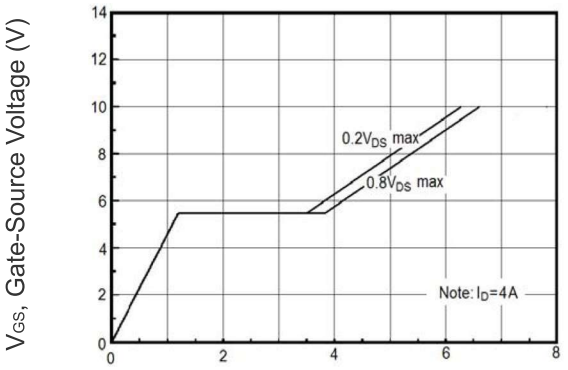


Figure 9 Gate charge waveforms

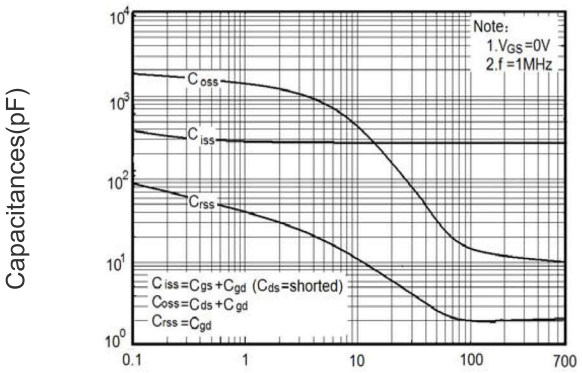


Figure 10 Capacitance

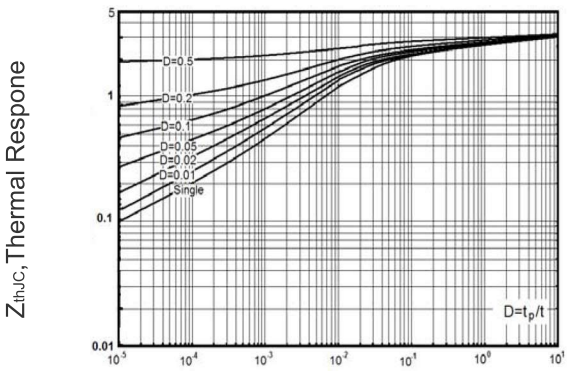
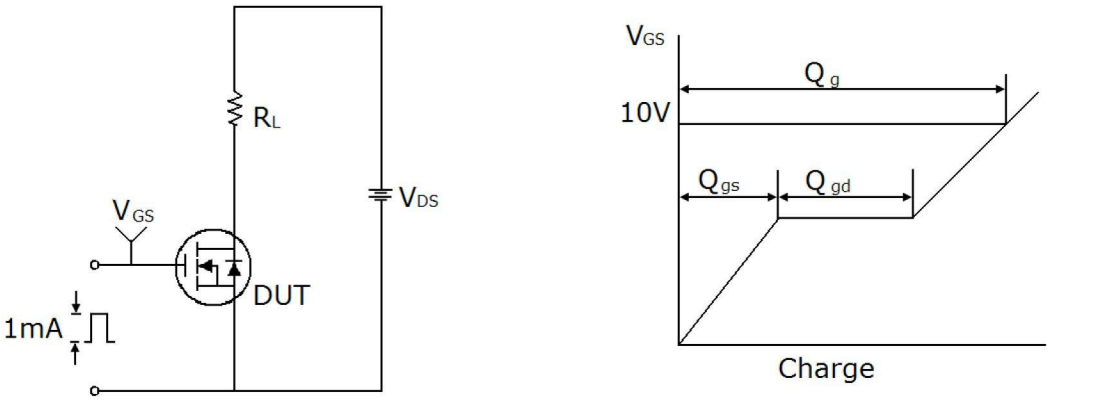
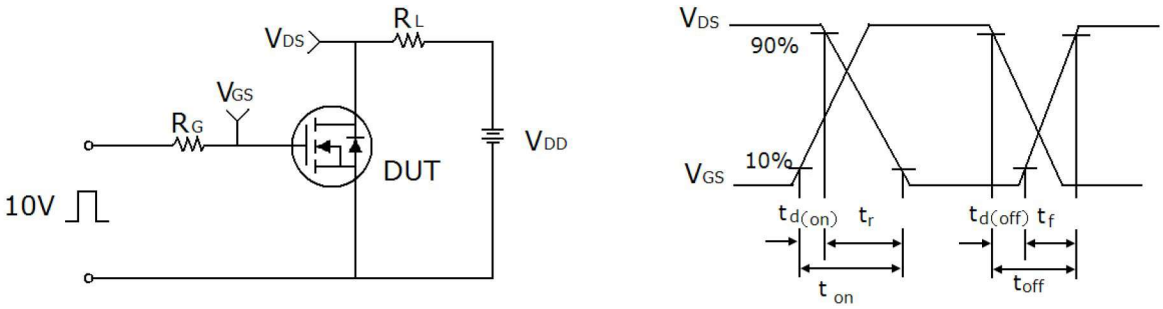


Figure 11 Transient Thermal Impedance

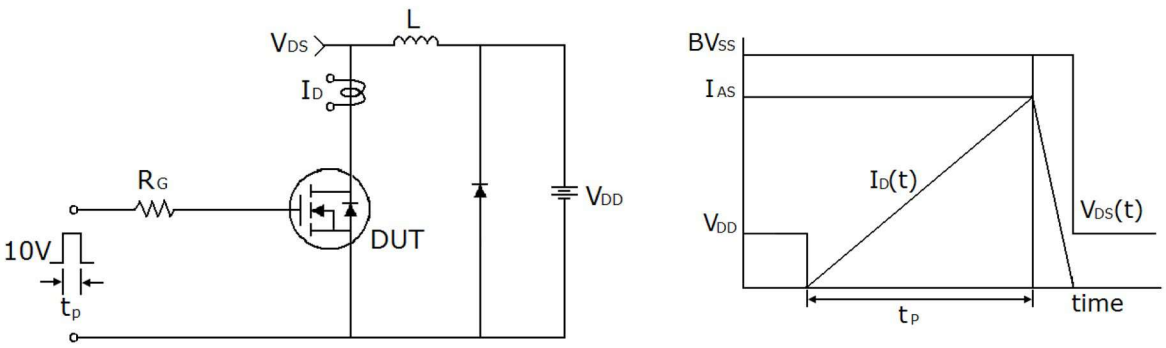
Test circuit



Gate charge test circuit & Waveform

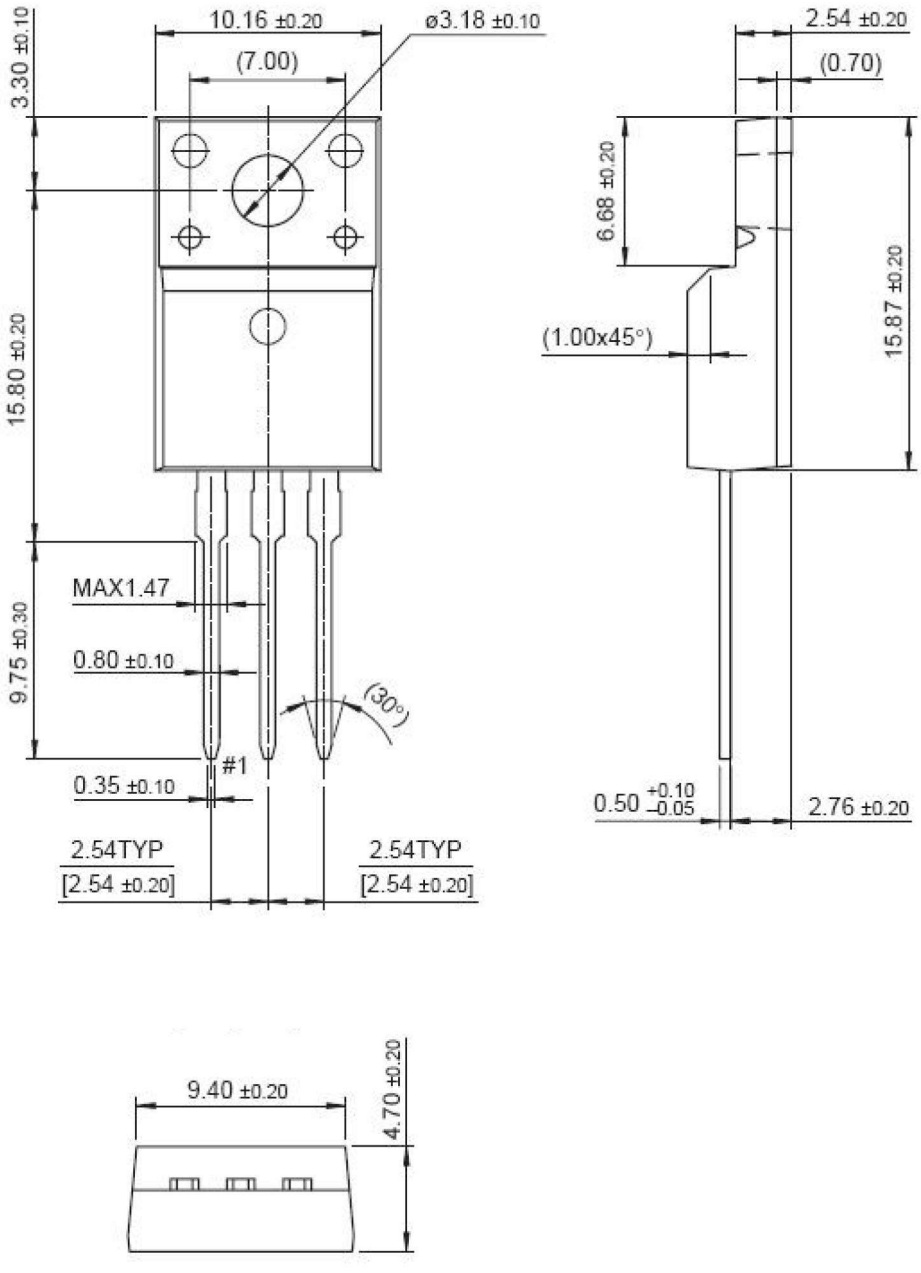


Switch Time Test Circuit



Unclamped Inductive Switching Test Circuit & Waveforms

TO-220F Package Information



Dimensions in Millimeters

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