MJ N-Channel Enhancement Mode Power MOSFET

Description

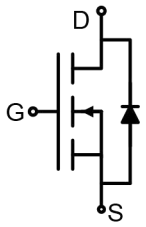
The MJ70N100I uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

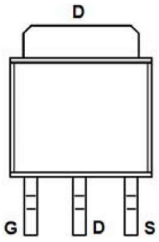
- V_{DS} =100V,I_D =57A
  $R_{DS(ON)}$ <16mΩ @ V_{GS}=10V (Typ:12mΩ)
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

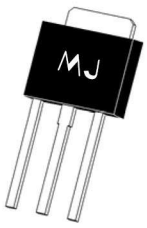
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-251 top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ70N100I	MJ70N100I	TO-251-3L	-	-	-

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	57	A
Drain Current-Continuous(T_C =100℃)	$I_{D(100℃)}$	40	A
Pulsed Drain Current	I_{DM}	190	A
Maximum Power Dissipation	P_D	170	W
Single pulse avalanche energy (Note 5)	E_{AS}	342	mJ
Derating factor		1.13	W/℃
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.88	℃/W

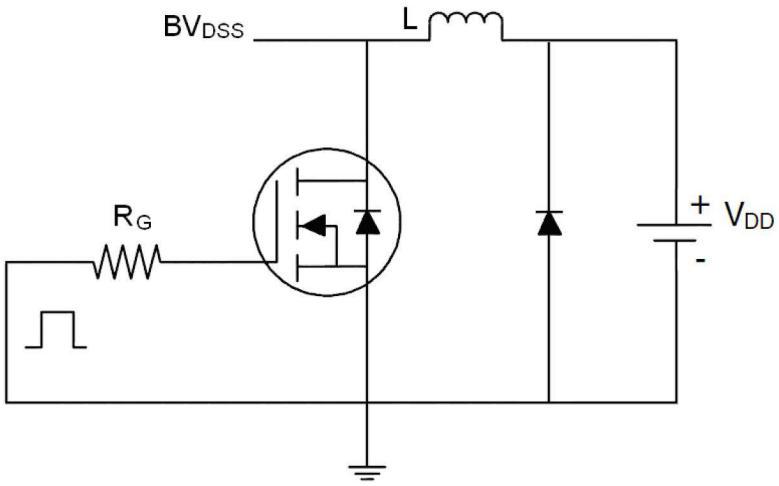
Electrical Characteristics (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=250μA	1.2	1.5	1.8	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	12	16	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	32	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V F=1.0MHz	-	4118	-	PF
Output Capacitance	C_{oss}		-	210	-	PF
Reverse Transfer Capacitance	C_{rss}		-	169	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V,I_D=20A V_{GS}=10V,R_{GEN}=2.5Ω	-	12	-	nS
Turn-on Rise Time	t_r		-	55	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	47	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=20A V_{GS}=10V	-	111	-	nC
Gate-Source Charge	Q_{gs}		-	11.5	-	nC
Gate-Drain Charge	Q_{gd}		-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	57	A
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=20A di/dt=100A/μs (Note 3)	-	36	-	nS
Reverse Recovery Charge	Q_{rr}		-	56	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

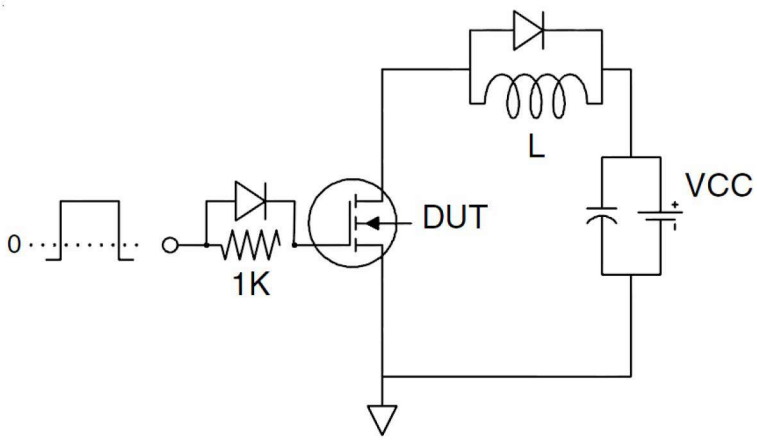
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition：Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

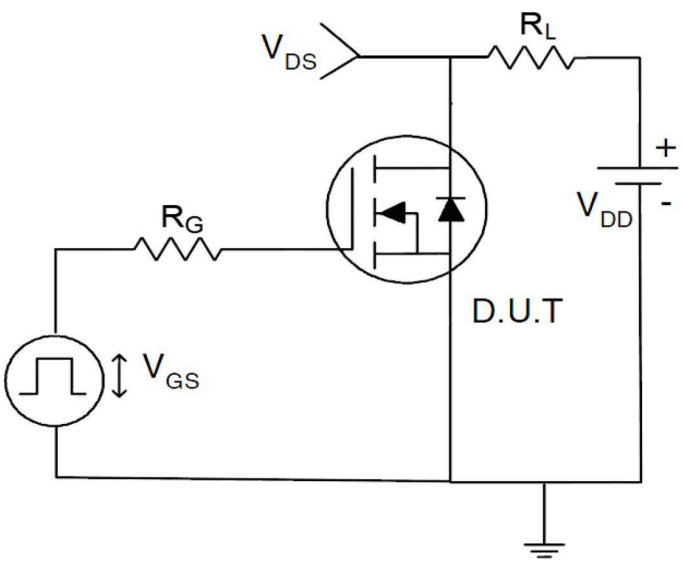
Test circuit



EAS test Circuit



Gate charge test Circuit



Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)

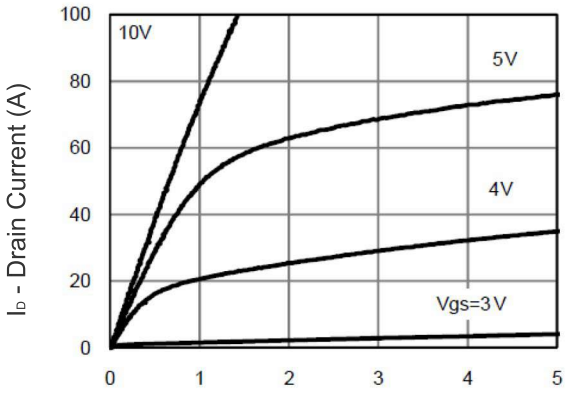


Figure 1 Output Characteristics

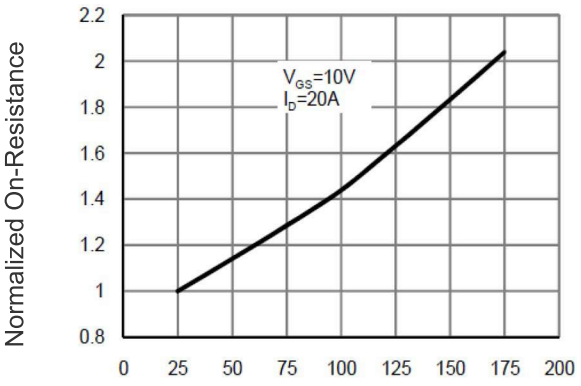


Figure 4 Rdson-Junction Temperature

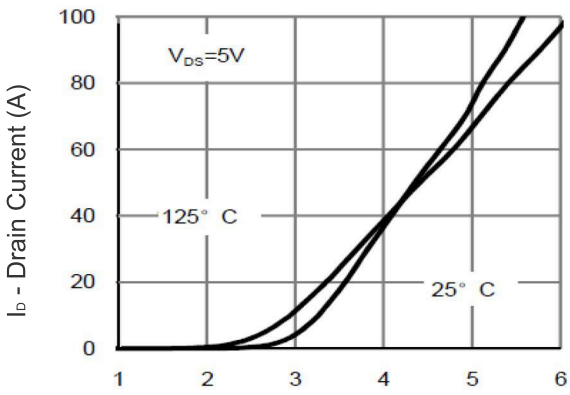


Figure 2 Transfer Characteristics

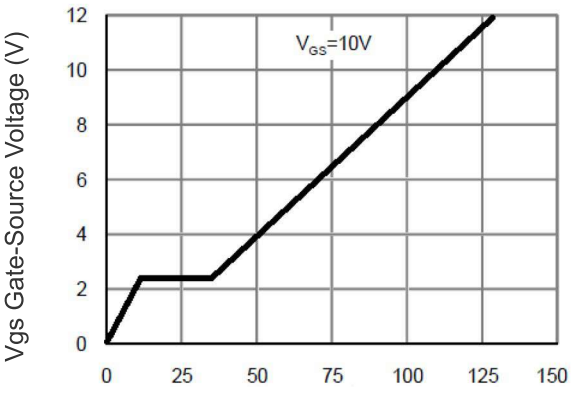


Figure 5 Gate Charge

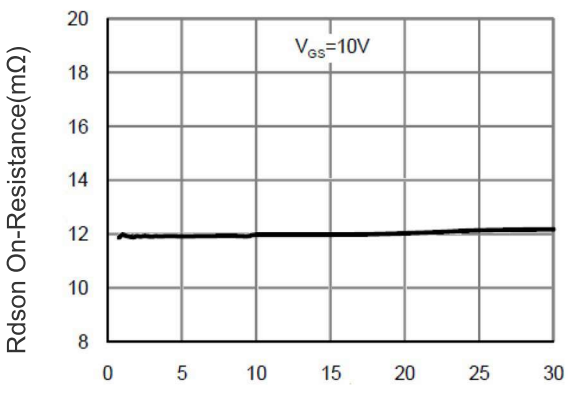


Figure 3 Rdson- Drain Current

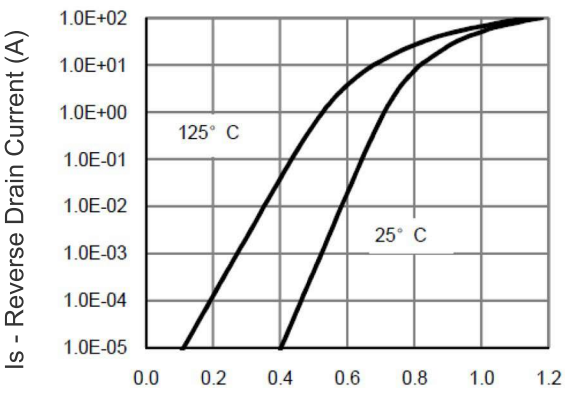


Figure 6 Source- Drain Diode Forward

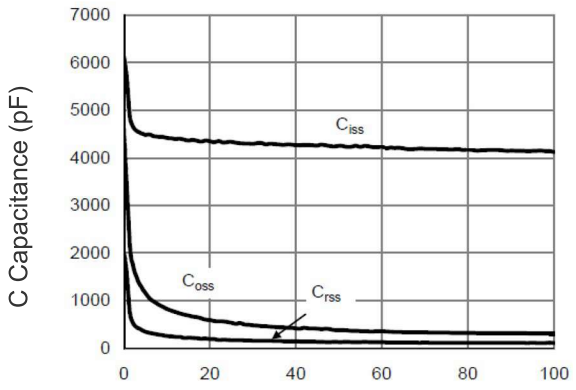


Figure 7 Capacitance vs Vds

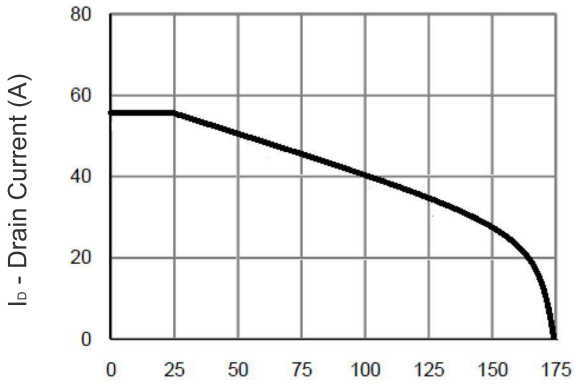


Figure 9 I_D Current De-rating

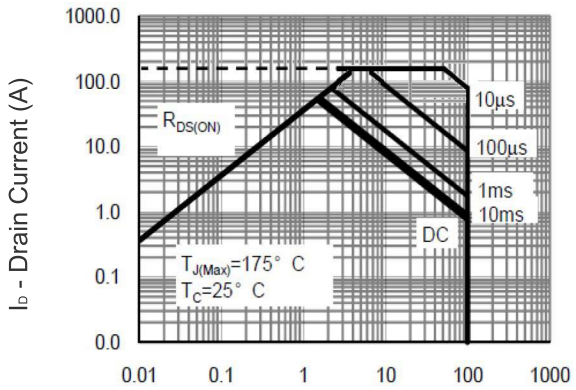


Figure 8 Safe Operation Area

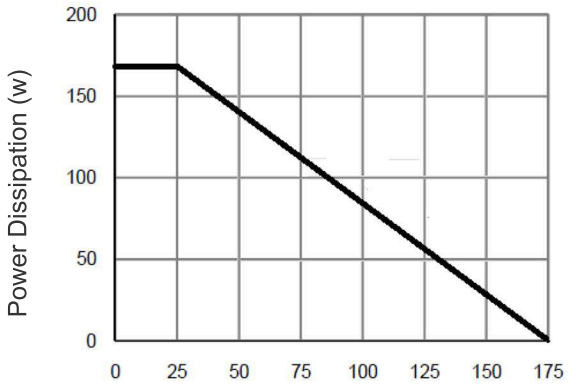


Figure 10 Power De-rating

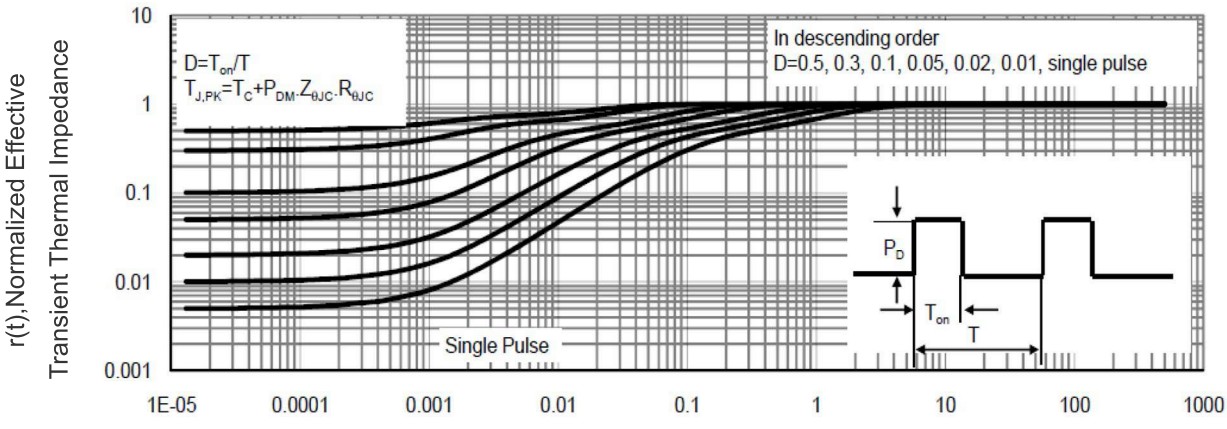
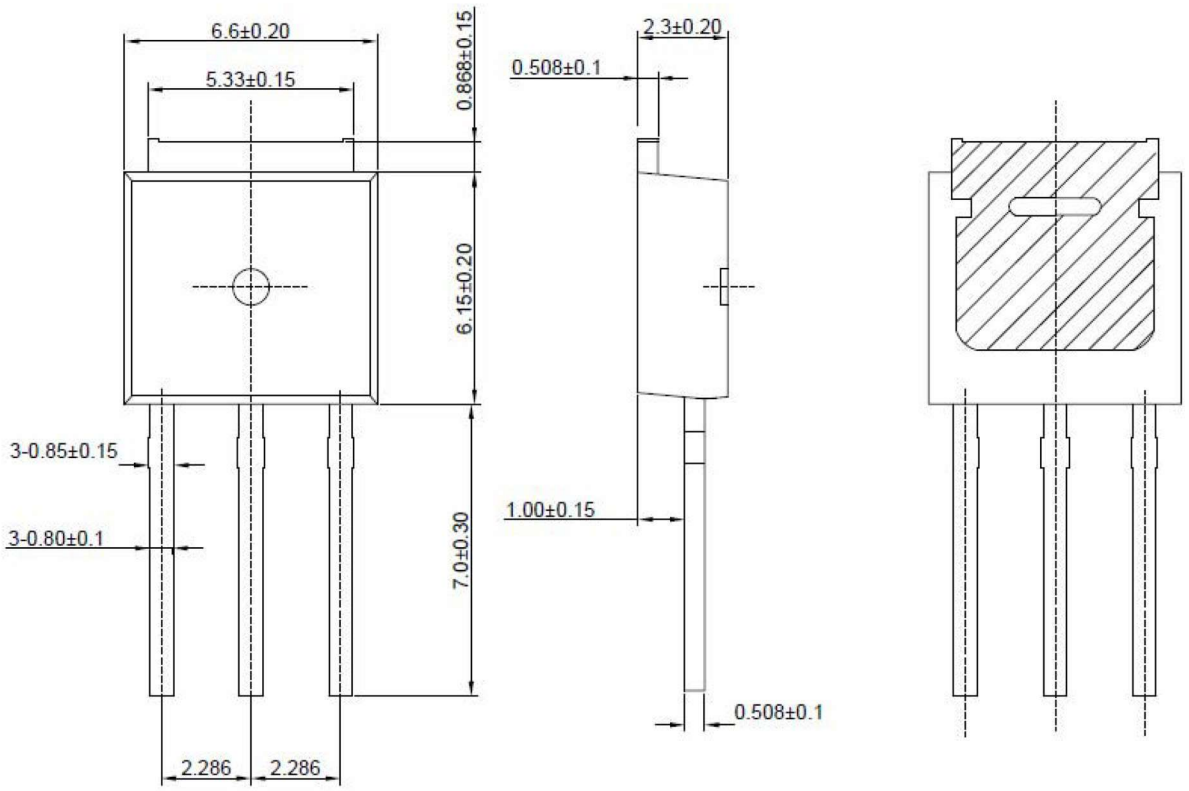
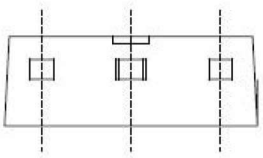


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-251 Package Information





1:塑封体为光面RA=0.2
2:未标注公差部分为±0.15mm

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