

MJ P-Channel Enhancement Mode Power MOSFET

Description

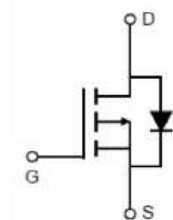
The MJ60P16AK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for use as a load switch or in PWM applications.

General Features

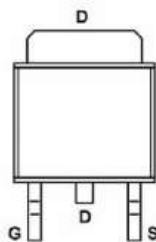
- ◆ $V_{DS} = -60V, I_D = -16A$
 $R_{DS(ON)} < 65m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 85m\Omega @ V_{GS} = -4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Excellent package for good heat dissipation

Application

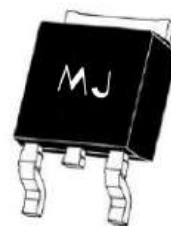
- ◆ Load switch
- ◆ PWM application



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ60P16AK	MJ60P16AK	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-16	A
Pulsed Drain Current	I_{DM}	-64	A
Maximum Power Dissipation	P_D	32	W
Derating factor		0.21	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	65	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	4.68	$^\circ\text{C/W}$
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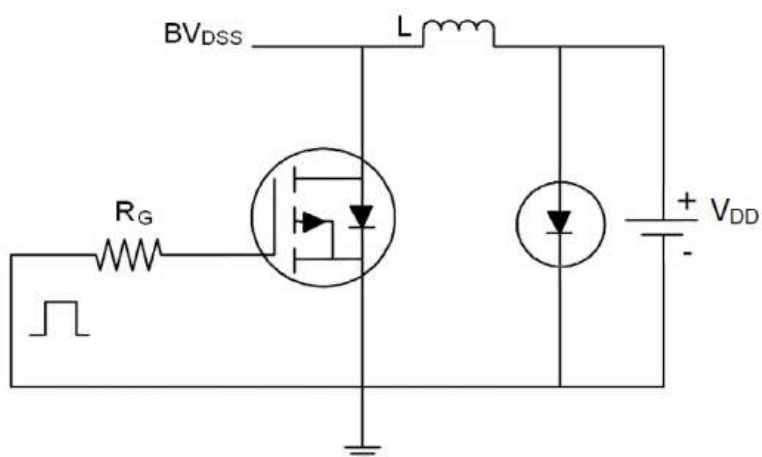
Electrical Characteristics (T_c =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1.0	-1.5	-2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-8A	-	55	65	mΩ
		V _{GS} =-4.5V, I _D =-8A	-	65	85	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V,I _D =-8A	-	15	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =-30V,V _{GS} =0V F=1.0MHz	-	1108	-	PF
Output Capacitance	C _{oss}		-	73.7	-	PF
Reverse Transfer Capacitance	C _{rss}		-	58.2	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V, R _L =3.75Ω V _{GS} =-10V,R _G =3Ω	-	8	-	nS
Turn-on Rise Time	t _r		-	4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	32	-	nS
Turn-Off Fall Time	t _f		-	7	-	nS
Total Gate Charge	Q _g	V _{DS} =-30V,I _D =-8A V _{GS} =-10V	-	23.4	-	nC
Gate-Source Charge	Q _{gs}		-	4.1	-	nC
Gate-Drain Charge	Q _{gd}		-	4.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =-16A	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	-16	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =-8A di/dt=-100A/μs <small>(Note 3)</small>	-	25	-	nS
Reverse Recovery Charge	Q _{rr}		-	31	-	nC

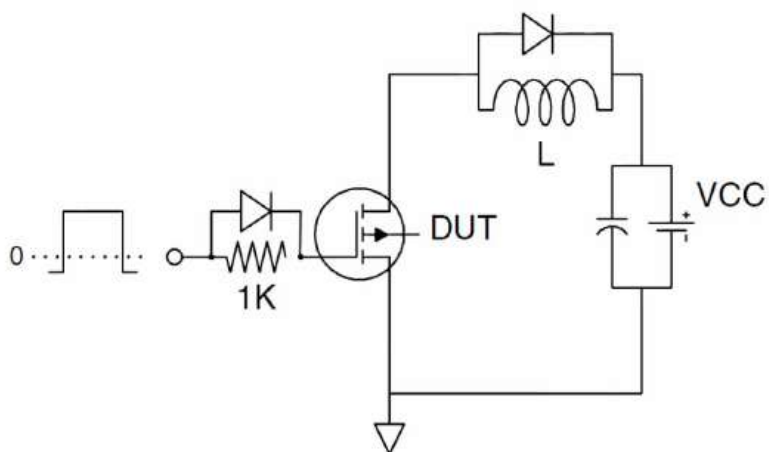
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production

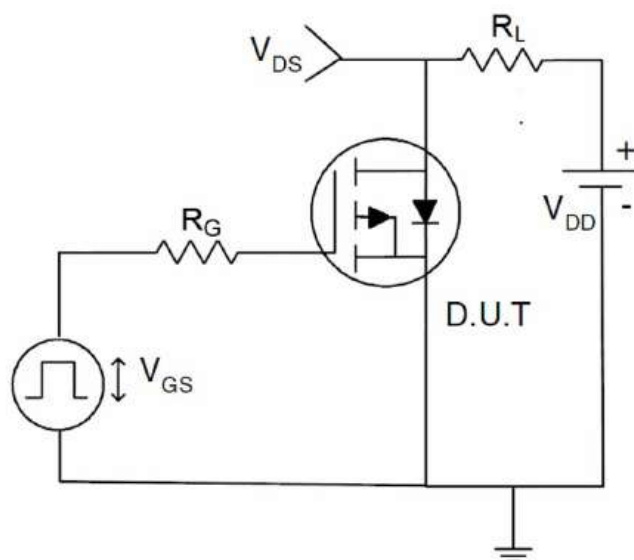
Test circuit



EAS test Circuit

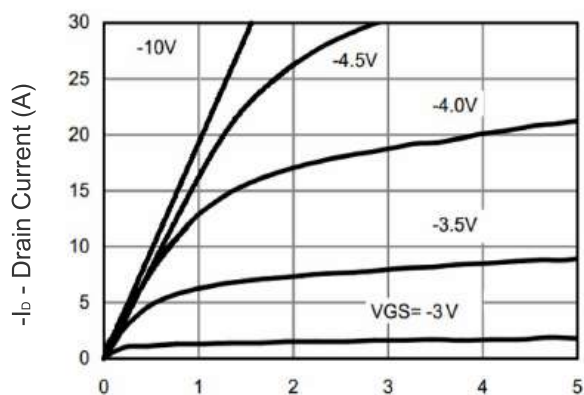


Gate charge test Circuit



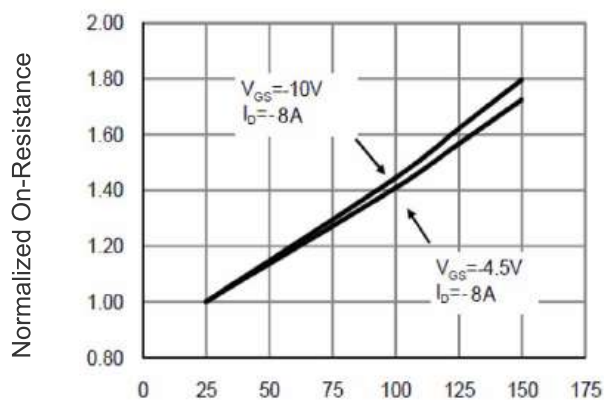
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



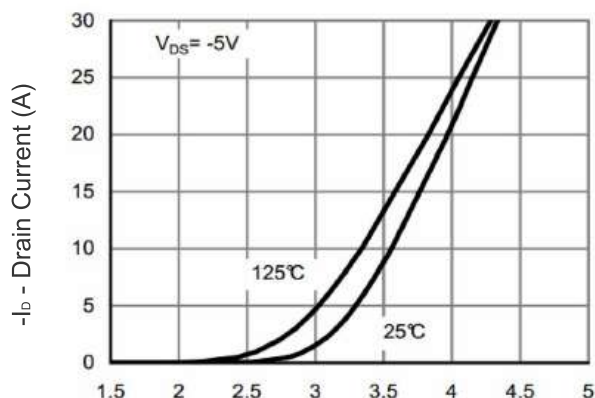
-V_{DS} Drain-Source Voltage (V)

Figure 1 Output Characteristics



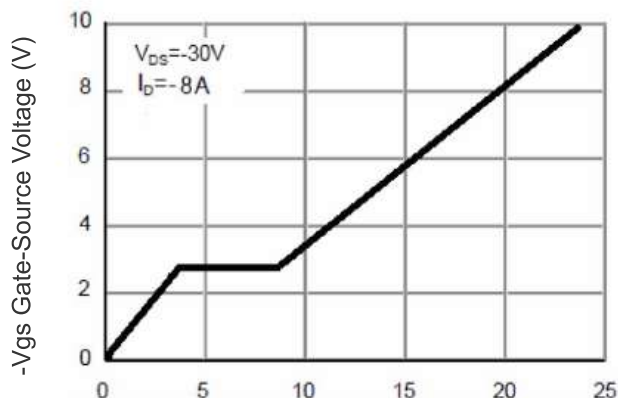
T_J -Junction Temperature(°C)

Figure 4 R_{DS(on)}-Junction Temperature



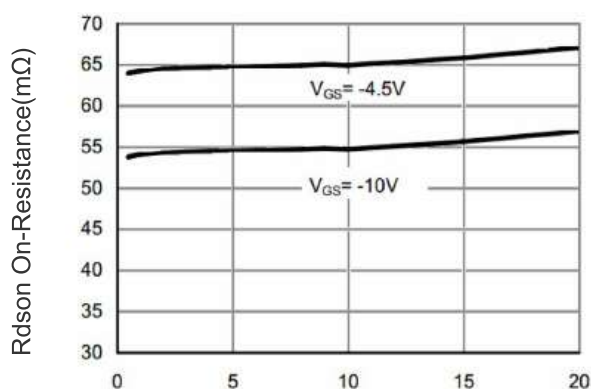
-V_{GS} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



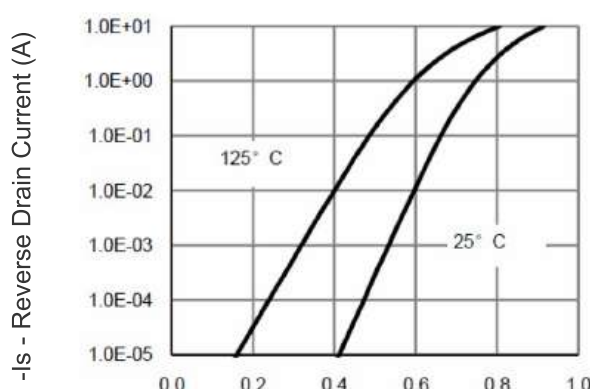
Q_g Gate Charge (nC)

Figure 5 Gate Charge



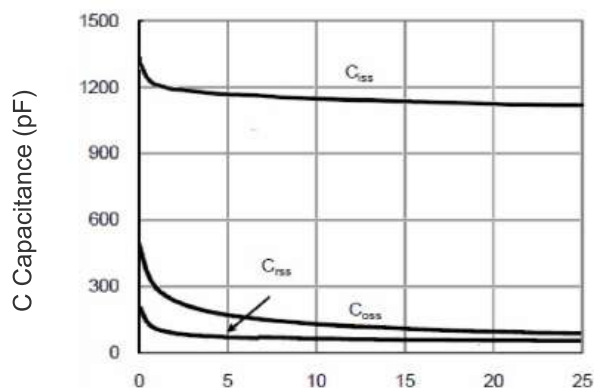
-I_D - Drain Current (A)

Figure 3 R_{DS(on)}- Drain Current

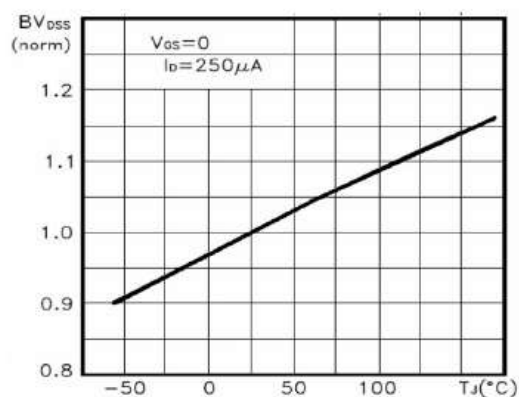


-V_{SD} Source-Drain Voltage (V)

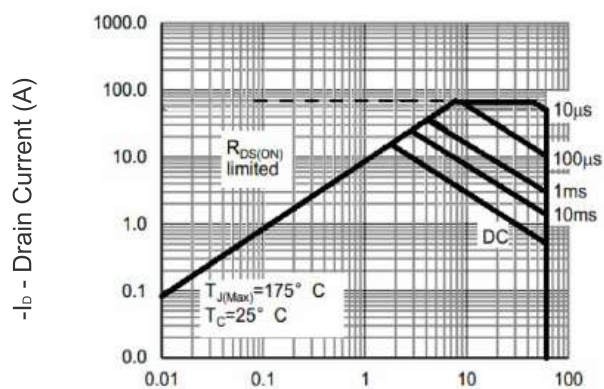
Figure 6 Source- Drain Diode Forward



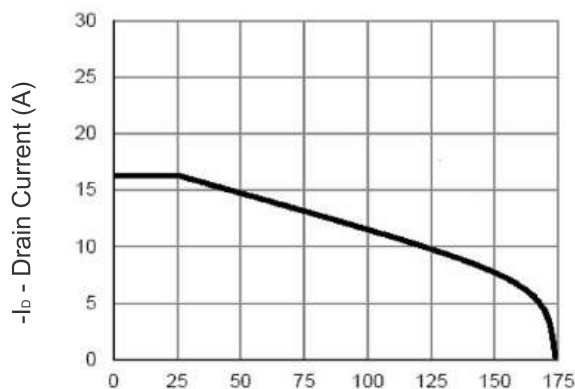
-Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



TJ -Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



-Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



TJ -Junction Temperature(°C)
Figure 10 Id Current De-rating

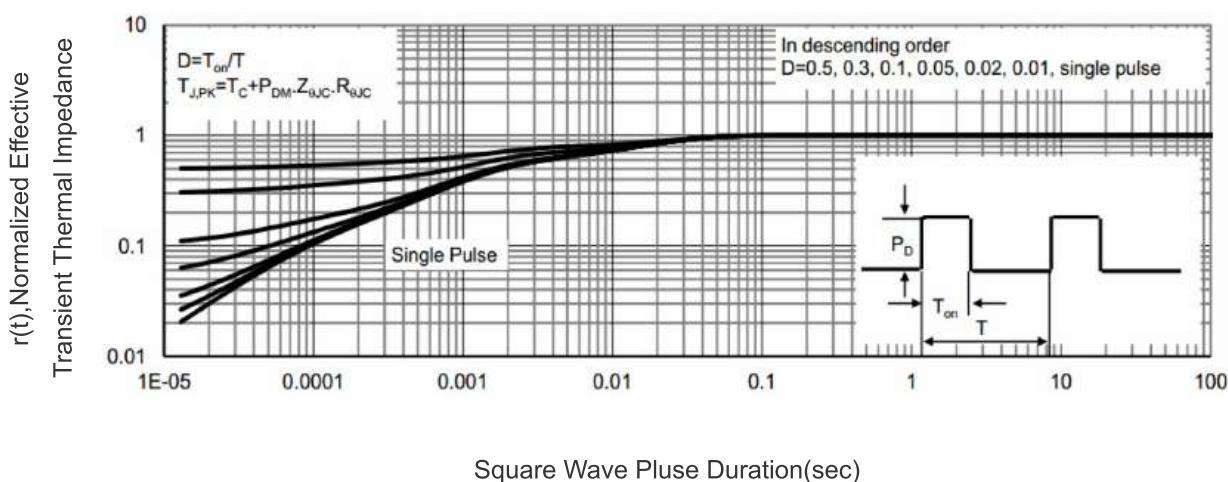
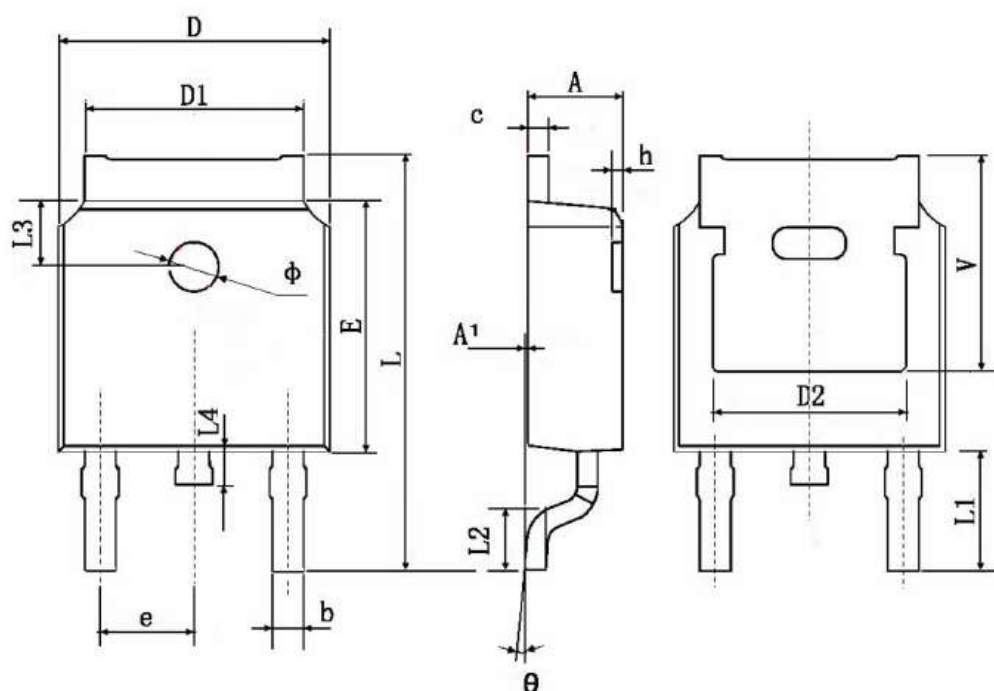


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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