MJ P-Channel Enhancement Mode Power MOSFET

Description

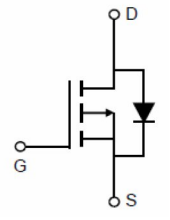
The MJ60P02Y uses advanced trench technology and design to provide excellent R DS(ON) with low gate charge. This device is well suited for use as a load switch or in PWM applications.

General Features

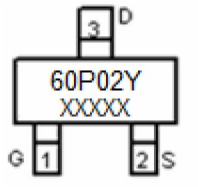
- V_{DS} =-60V,I_D =-2A
- $R_{DS(ON)}$ <160mΩ @ V_{GS} =-10V
- $R_{DS(ON)}$ <200mΩ @ V_{GS} =-4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

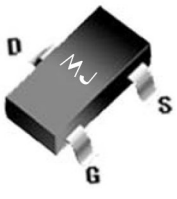
- Load switch
- PWM application



Schematic diagram



Marking and pin assignment



SOT-23-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
60P02Y	MJ60P02Y	SOT23-3L	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{DS}	±20	V
Drain Current-Continuous	I_D	-2	A
Pulsed Drain Current (Note 1)	I_{DM}	-8	A
Maximum Power Dissipation	P_D	1.7	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	73.5	℃/W

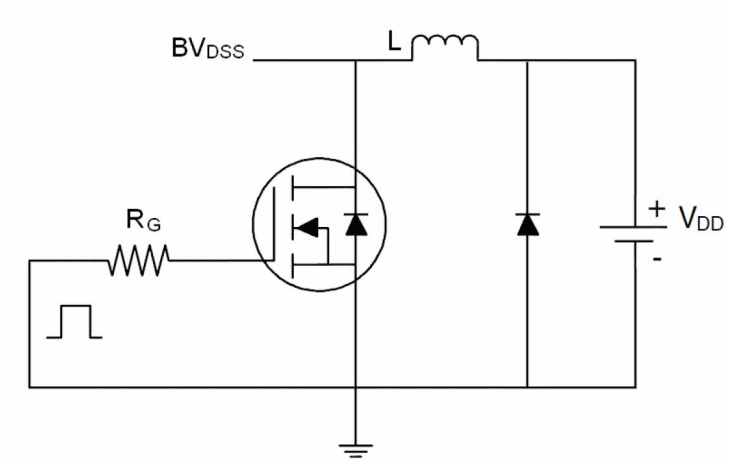
Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V I_D =250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =-60V,V_{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS} =±20V,V_{GS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS} ,I_D =250μA	-1.4	-2.0	-2.6	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} =-10V, I_D =-2A	-	140	160	mΩ
		V_{GS} =-4.5V, I_D =-2A	-	160	200	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-5V,I_D =-2A	-	3	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS} =-30V,V_{GS} =0V, F=1.0MHz	-	452	-	PF
Output Capacitance	C_{oss}		-	27.8	-	PF
Reverse Transfer Capacitance	C_{rss}		-	21.5	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD} =-30V, ,R_L =-2Ω V_{GS} =-10V,R_{GEN} =3Ω	-	40	-	nS
Turn-on Rise Time	t_r		-	35	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS} =-30V,I_D =-2A, V_{GS} =-10V	-	9.0	-	nC
Gate-Source Charge	Q_{gs}		-	1.6	-	nC
Gate-Drain Charge	Q_{gd}		-	1.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS} =0V,I_S =-2A	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-2	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F =- 2A di/dt = -100A/μs (Note3)	-	25		nS
Reverse Recovery Charge	Q_{rr}		-	31		nC

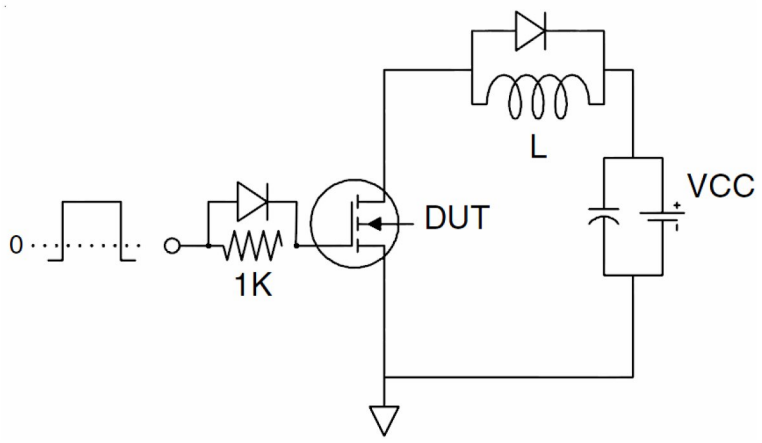
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production

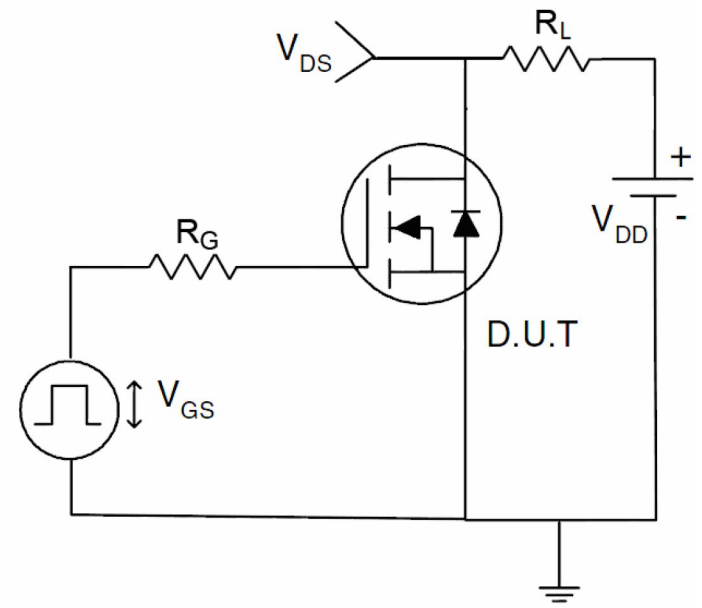
Test Circuit



EAS test Circuit



Gate charge test Circuit



Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)

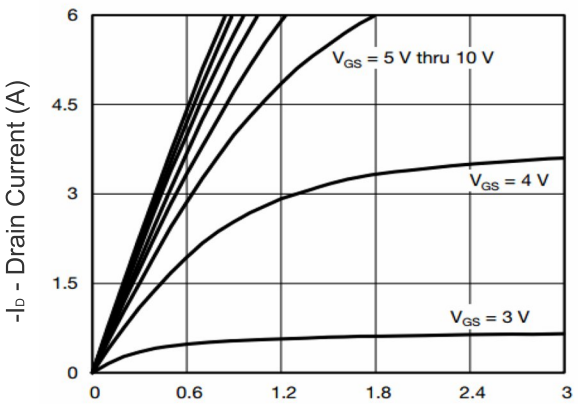


Figure 1 Output Characteristics

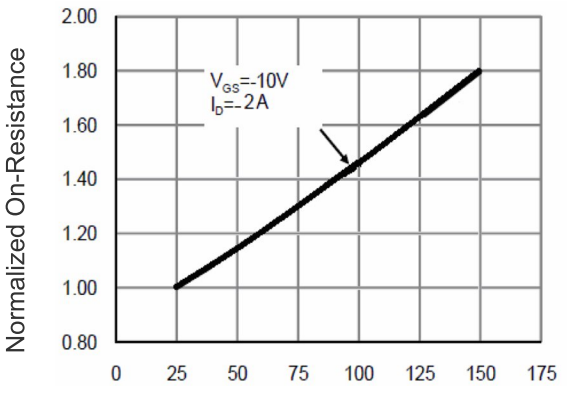


Figure 4 Rdson-Junction Temperature

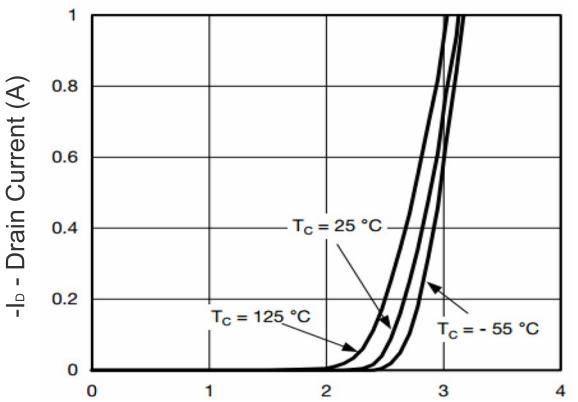


Figure 2 Transfer Characteristics

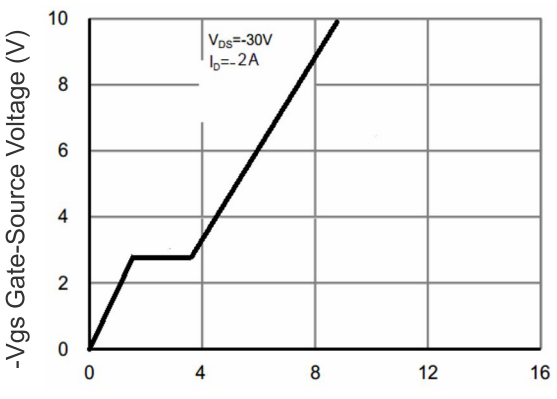


Figure 5 Gate Charge

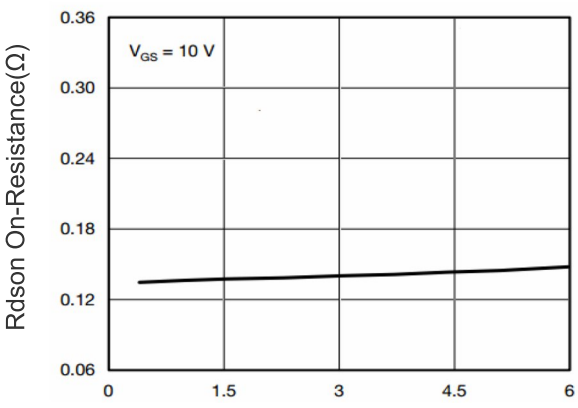


Figure 3 Rdson- Drain Current

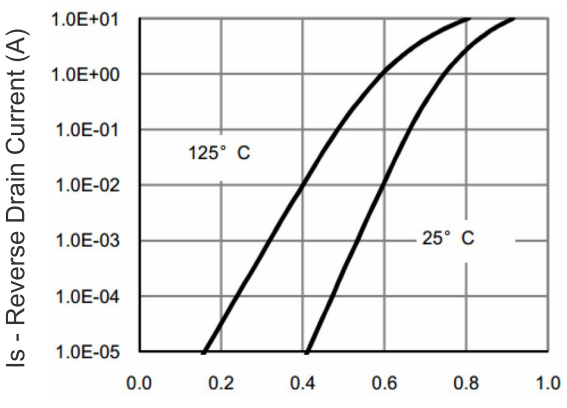
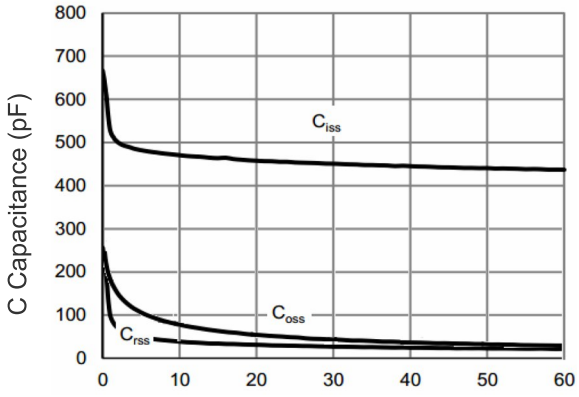
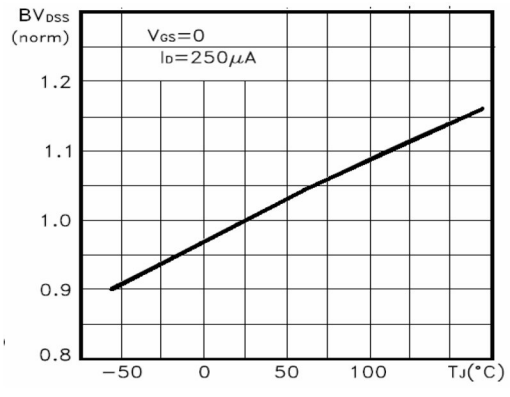


Figure 6 Source- Drain Diode Forward



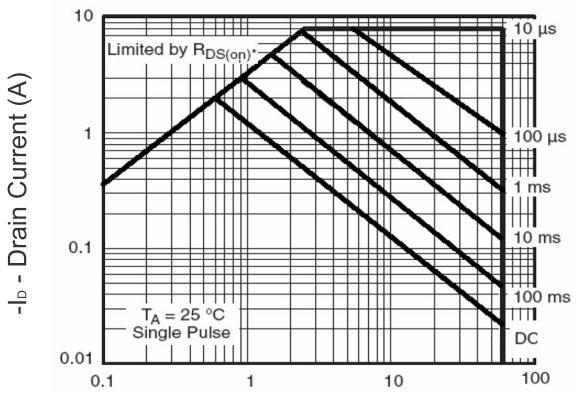
-Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



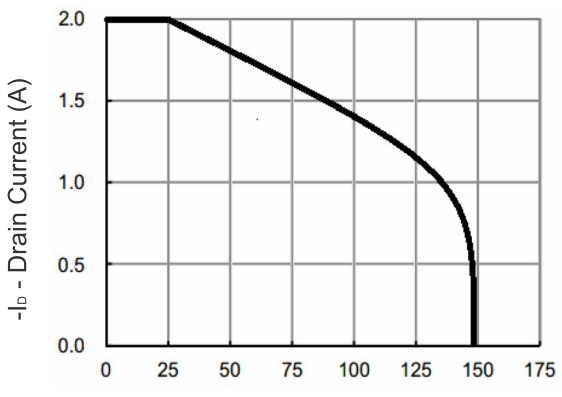
TJ -Junction Temperature(℃)

Figure 9 BVDSS vs Junction Temperature



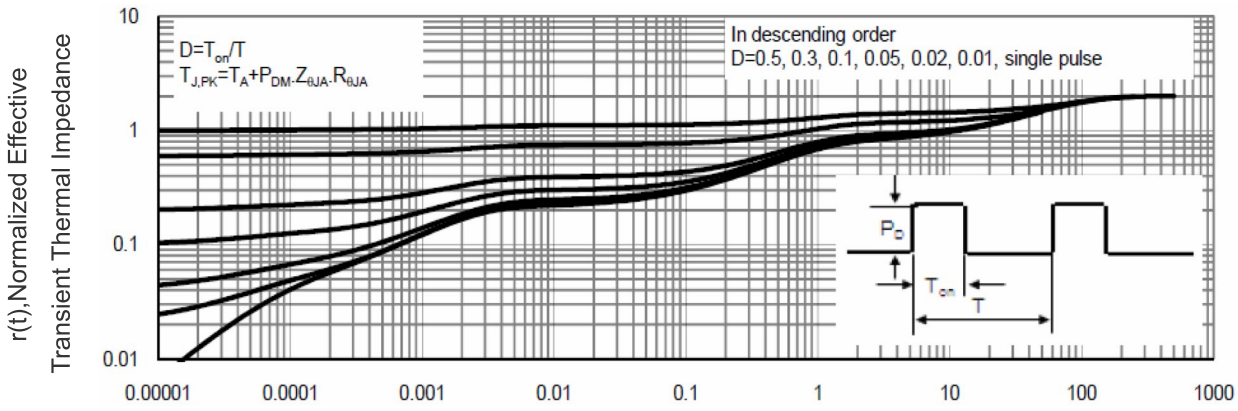
-Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ -Junction Temperature(℃)

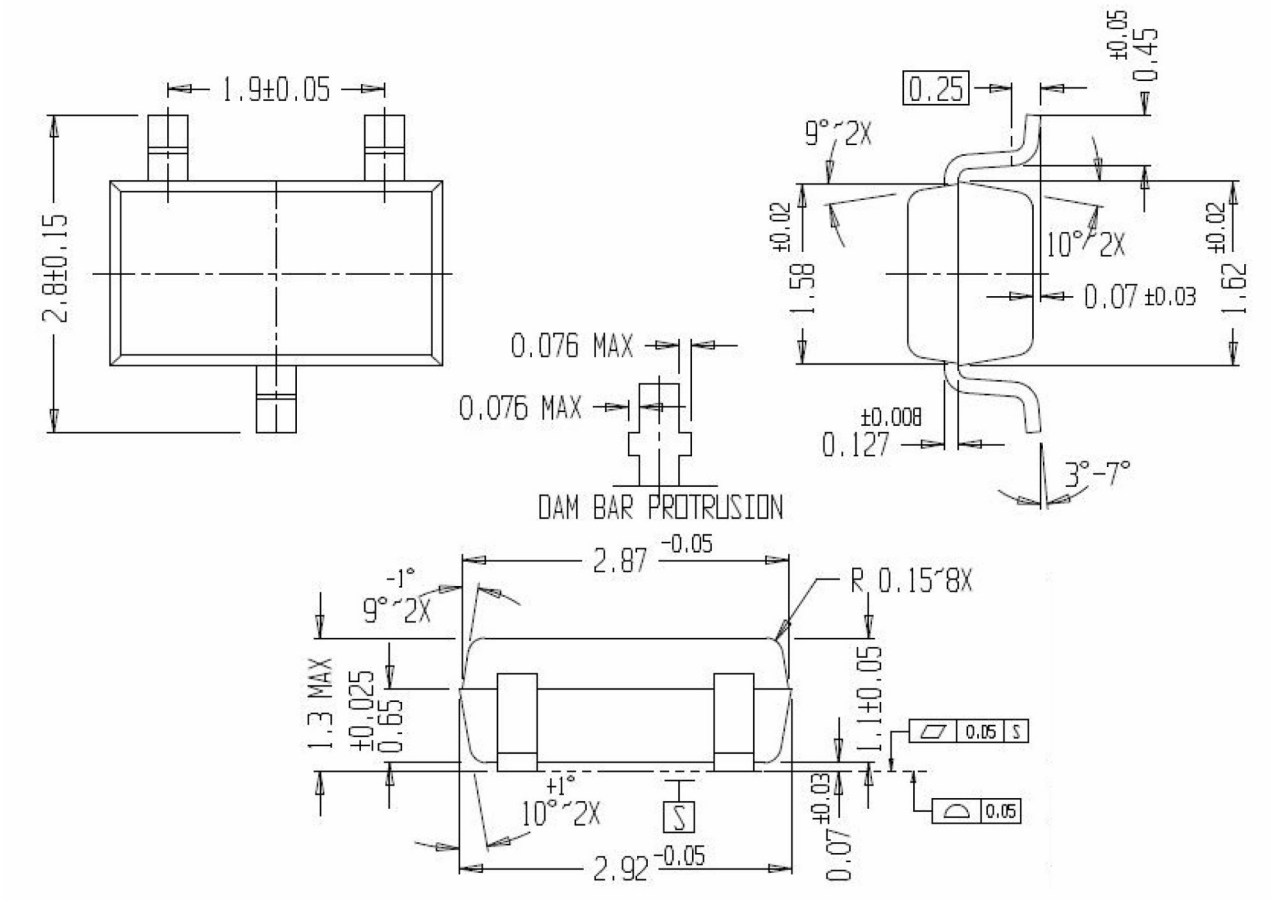
Figure 10 ID Current De-rating



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

SOT23-3L Package Information



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