



# MJ N-Channel Enhancement Mode Power MOSFET

## Description

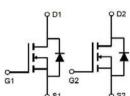
The MJ60ND09AS uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

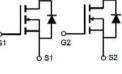
#### **General Features**

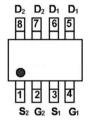
- ♦ Vps =60V.lp =9A  $R_{DS(ON)}$  <15m $\Omega$  @ V<sub>GS</sub>=10V  $(Typ:10m\Omega)$  $R_{DS(ON)}$  <18m $\Omega$  @ Vgs=4.5V  $(Typ:14m\Omega)$
- ♦ High density cell design for ultra low Rdson
- ◆ Fully characterized avalanche voltage and current
- ◆ Low gate to drain charge to reduce switching losses

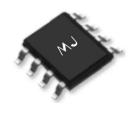
## **Application**

- Power switching application
- Load switch









Schematic diagram

Marking and pin Assignment

SOP-8 top view

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ60ND09AS	MJ60ND09AS	SOP-8	-	-	-

### Absolute Maximum Ratings (Tc=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	60	V
Gate-Source Voltage	Vgs	±20	V
Drain Current-Continuous	lD	9	Α
Drain Current-Continuous(Tc =100°C)	ID(100°C)	6.4	А
Pulsed Drain Current	Ірм	36	А
Maximum Power Dissipation	PD	2.6	W
Operating Junction and Storage Temperature Range	Тл,Тsтg	-55 To 150	°C

#### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	RөJA	48	°C/W
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# Electrical Characteristics (Tc=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	'		ı			
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V I <sub>D</sub> =250µA	60	_	-	V
Zero Gate Voltage Drain Current	loss	Vps=60V,Vgs=0V	-	-	1	μΑ
Gate-Body Leakage Current	lgss	V <sub>DS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	VGS(th)	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250µA	1.2	1.8	2.2	V
Davis Octobe Desistance	D	V <sub>GS</sub> =10V, I <sub>D</sub> =9A	-	10	15	mΩ
Drain-Source On-State Resistance	Rds(on)	V <sub>GS</sub> =4.5V, I <sub>D</sub> =9A		14	18	mΩ
Forward Transconductance	grs	V <sub>DS</sub> =5V,I <sub>D</sub> =9A	25	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	Clss		-	2180	-	PF
Output Capacitance	Coss	V <sub>DS</sub> =30V,V <sub>GS</sub> =0V F=1.0MHz	-	350	-	PF
Reverse Transfer Capacitance	Crss	•	-	270	-	PF
Switching Characteristics (Note 4)	'		ı			
Turn-on Delay Time	t <sub>d(on)</sub>		-	8.5	-	nS
Turn-on Rise Time	tr	VDD=30V, RL=1Ω	-	6	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}=10V,R_{G}=3\Omega$	_	30	-	nS
Turn-Off Fall Time	tr		-	5	-	nS
Total Gate Charge	Qg		-	58	-	nC
Gate-Source Charge	Qgs	V <sub>DS</sub> =30V,I <sub>D</sub> =9A V <sub>GS</sub> =10V	-	8	-	nC
Gate-Drain Charge	Qgd		_	17	_	nC
Drain-Source Diode Characteristics				<u> </u>		<u> </u>
Diode Forward Voltage (Note 3)	Vsp	V <sub>GS</sub> =0V,I <sub>S</sub> =9A	-	_	1.2	V
Diode Forward Current (Note 2)	Is		-	_	9	Α
Reverse Recovery Time	trr		_	30	_	nS
Reverse Recovery Charge	Qrr	TJ=25°C, IF=9A di/dt=100A/µs <sup>(Note 3)</sup>	_	44	_	nC
Ttovorco recovery onarge	QIT .			77		110

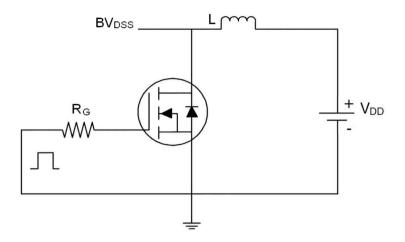
### Notes:

- $\textcircled{1} \ \ \mathsf{Repetitive} \ \ \mathsf{Rating:} \ \ \mathsf{Pulse} \ \ \mathsf{width} \ \ \mathsf{limited} \ \ \mathsf{by} \ \ \mathsf{maximum} \ \mathsf{junction} \ \ \mathsf{temperature}.$
- ② Surface Mounted on FR4 Board,  $t \le 10$  sec.
- ③ Pulse Test: Pulse Width ≤ 300 $\mu$ s, Duty Cycle ≤ 2%.
- 4 Guaranteed by design, not subject to production
- $\begin{tabular}{ll} \hline (5) EAS condition: Tj=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, Rg=25\Omega \\ \hline \end{tabular}$

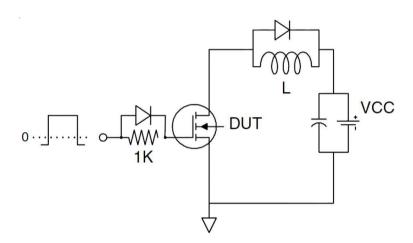




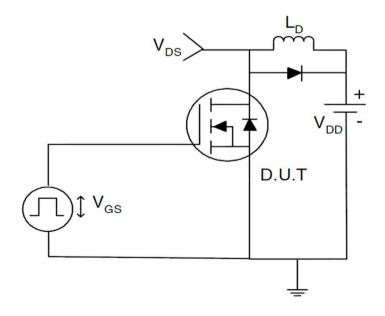
## Test circuit



Eas test Circuit



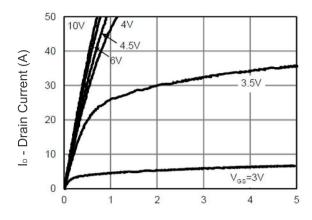
Gate charge test Circuit



Switch Time Test Circuit

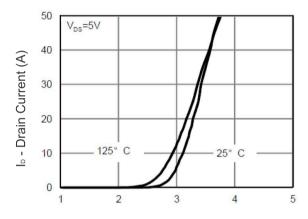


## Typical Electrical and Thermal Characteristics (Curves)

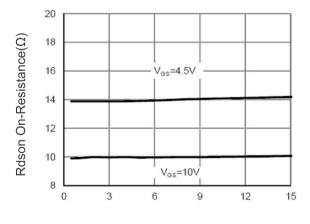


Vds Drain-Source Voltage (V)

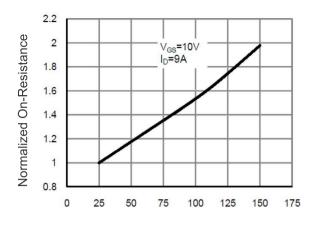
Figure 1 Output Characteristics



Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics

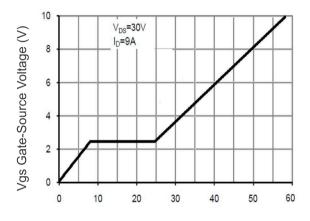


I<sub>D</sub> - Drain Current (A)
Figure 3 Rdson- Drain Current

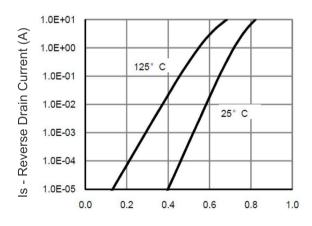


T<sub>J</sub> -Junction Temperature(°C)





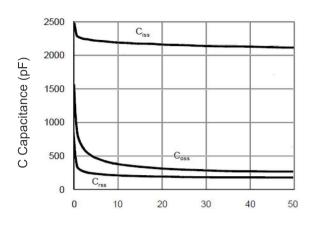
Qg Gate Charge (nC)
Figure 5 Gate Charge



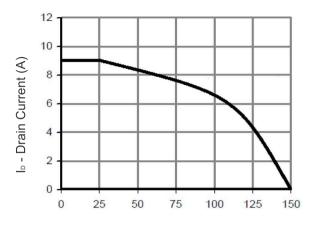
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

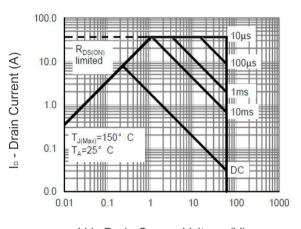




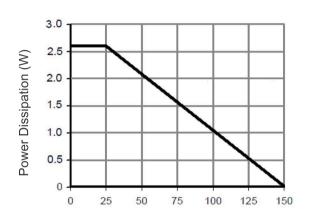
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



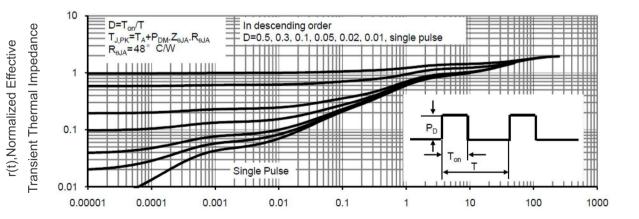
T<sub>J</sub> -Junction Temperature(°C)
Figure 9 Current De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T<sub>J</sub> -Junction Temperature(°C) Figure 10 Power De-rating



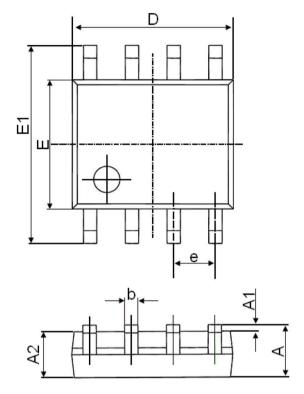
Square Wave Pluse Duration(sec)

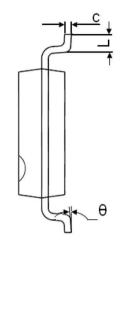
Figure 11 Normalized Maximum Transient Thermal Impedance





# SOP-8 Package Information





Symbol	Dimensions I	n Millimeters	Dimensions In Inches		
	Min.	Max.	Min.	Max.	
A	1.350	1.750	0.053	0.069	
A1	0.100	0.250	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
С	0.170	0.250	0.006	0.010	
D	4.700	5.100	0.185	0.200	
E	3.800	4.000	0.150	0.157	
E1	5.800	6.200	0.228	0.244	
е	1.270(BSC)		0.050(BSC)		
L	0.400	1.270	0.016	0.050	
θ	0°	8°	0°	8°	





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