

# MJ N-Channel Enhancement Mode Power MOSFET

## Description

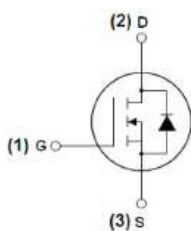
The MJ6080K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

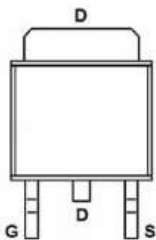
- ◆  $V_{DS} = 60V, I_D = 80A$   
 $R_{DS(ON)} < 8.5m\Omega @ V_{GS} = 10V$
- ◆ High density cell design for ultra low  $R_{dson}$
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high  $E_{AS}$
- ◆ Excellent package for good heat dissipation

## Application

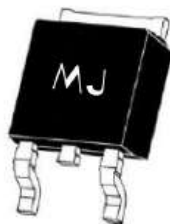
- ◆ PWM
- ◆ Load Switching



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100%  $\Delta V_{ds}$  TESTED!

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ6080K	MJ6080K	TO-252-2L	-	-	-

## Absolute Maximum Ratings ( $T_c = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	80	A
Drain Current-Continuous( $T_c = 100^{\circ}\text{C}$ )	$I_{D(100^{\circ}\text{C})}$	56.5	A
Pulsed Drain Current	$I_{DM}$	320	A
Maximum Power Dissipation	$P_D$	110	W
Derating factor		0.73	W/ $^{\circ}\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	390	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^{\circ}\text{C}$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.36	$^{\circ}\text{C/W}$
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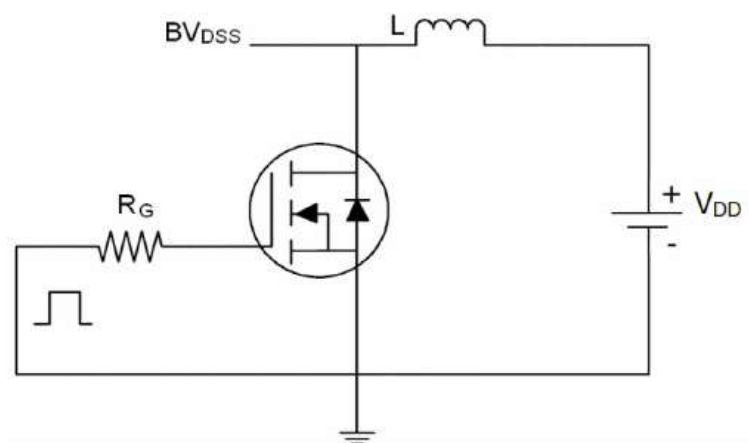
Electrical Characteristics (T<sub>c</sub> =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =±20V,V <sub>GS</sub> =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	2	2.8	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	7	8.5	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V,I <sub>D</sub> =20A	20	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V,V <sub>GS</sub> =0V F=1.0MHz	-	4000	-	PF
Output Capacitance	C <sub>oss</sub>		-	290	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	210	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, R <sub>L</sub> =1Ω V <sub>GS</sub> =10V,R <sub>G</sub> =3Ω	-	8.5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	7	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	40	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V,I <sub>D</sub> =20A V <sub>GS</sub> =10V	-	90	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	9	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	18	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I <sub>S</sub>		-	-	80	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> =25°C, I <sub>F</sub> =20A di/dt=100A/μs <small>(Note 3)</small>	-	32	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	45	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

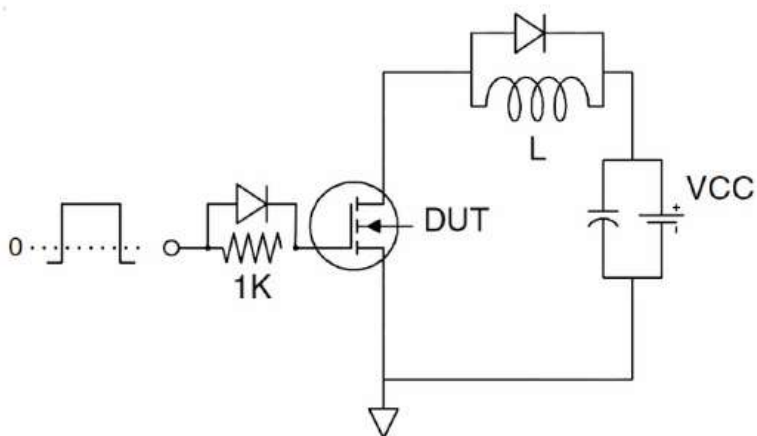
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T<sub>J</sub>=25℃,V<sub>DD</sub>=20V,V<sub>G</sub>=10V,L=0.5mH,R<sub>g</sub>=25Ω

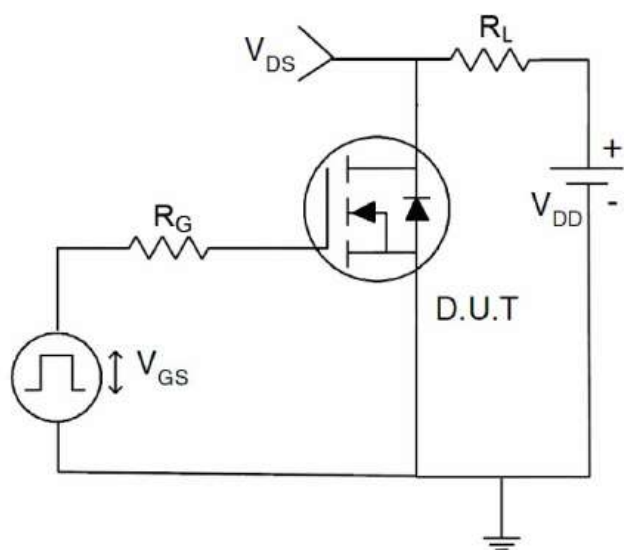
# Test circuit



EAS test Circuit

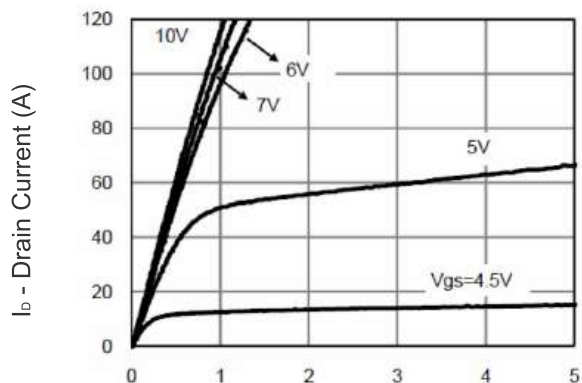


Gate charge test Circuit

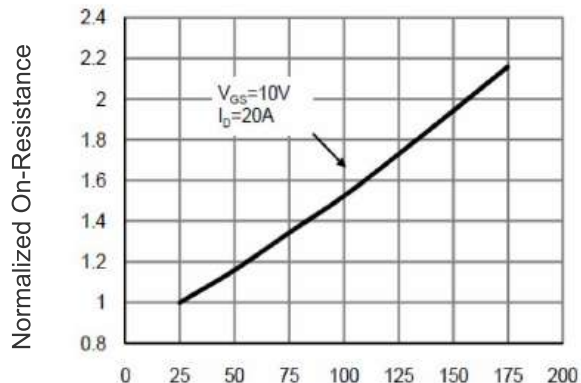


Switch Time Test Circuit

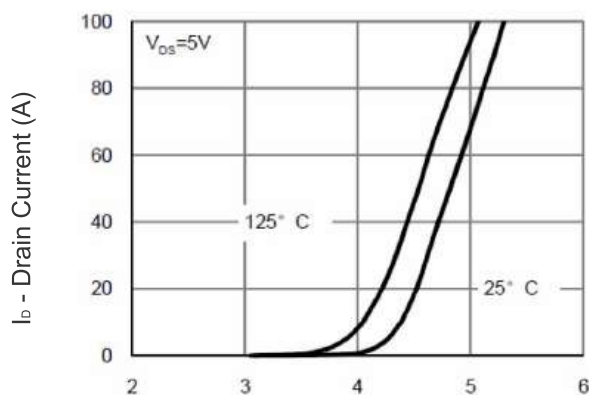
## Typical Electrical and Thermal Characteristics (Curves)



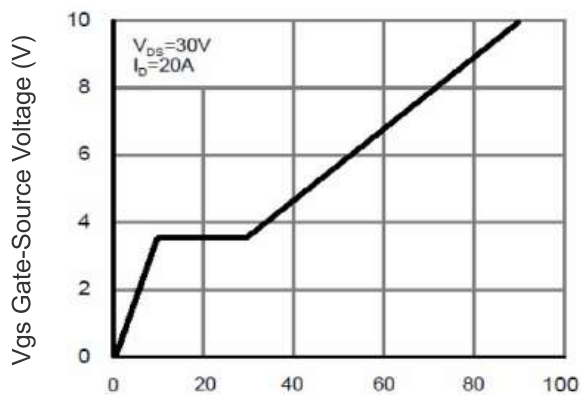
Vds Drain-Source Voltage (V)  
Figure 1 Output Characteristics



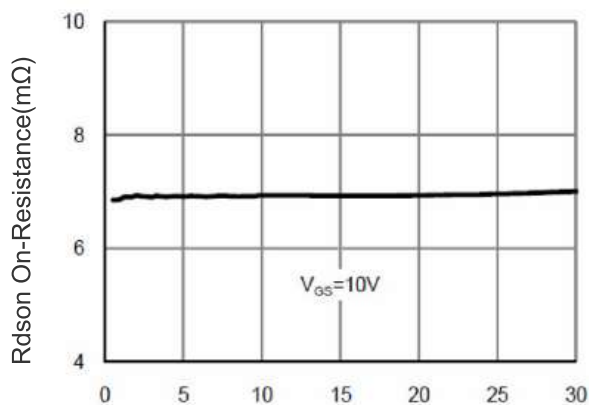
Tj -Junction Temperature(°C)  
Figure 4 Rdson-Junction Temperature



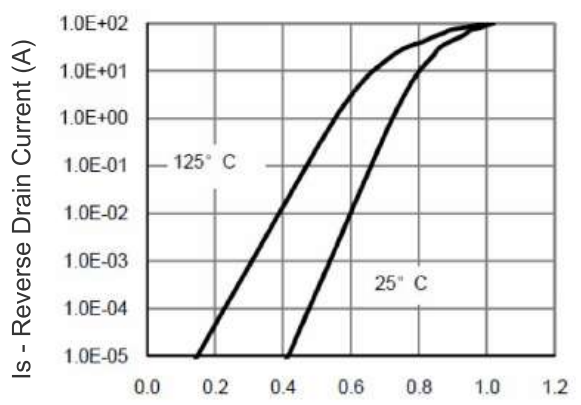
Vgs Gate-Source Voltage (V)  
Figure 2 Transfer Characteristics



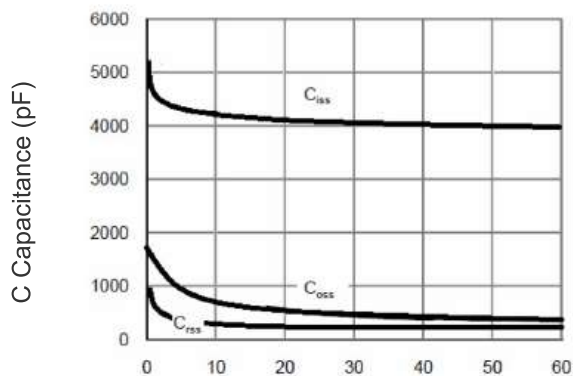
Qg Gate Charge (nC)  
Figure 5 Gate Charge



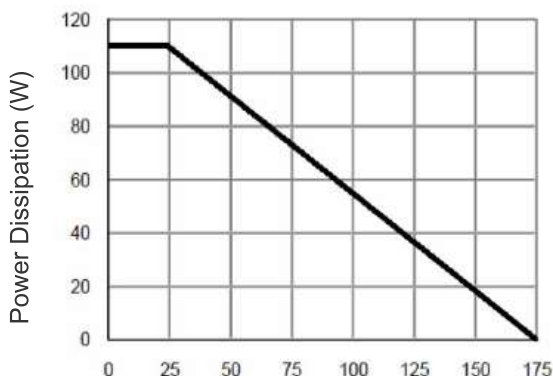
Id - Drain Current (A)  
Figure 3 Rdson- Drain Current



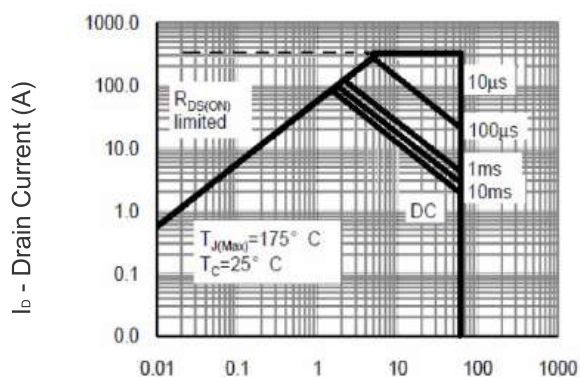
Vsd Source-Drain Voltage (V)  
Figure 6 Source- Drain Diode Forward



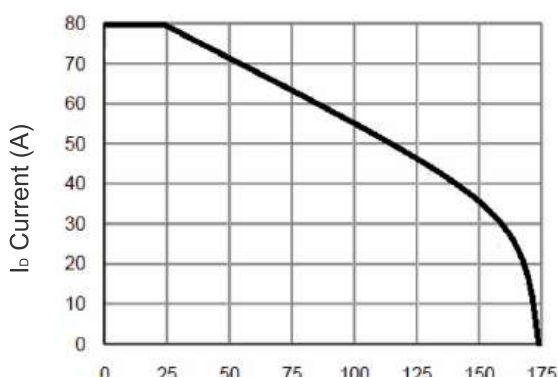
Vds Drain-Source Voltage (V)  
Figure 7 Capacitance vs Vds



TJ-Junction Temperature (°C)  
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)  
Figure 8 Safe Operation Area



TJ-Junction Temperature (°C)  
Figure 10 Id Current- Junction Temperature

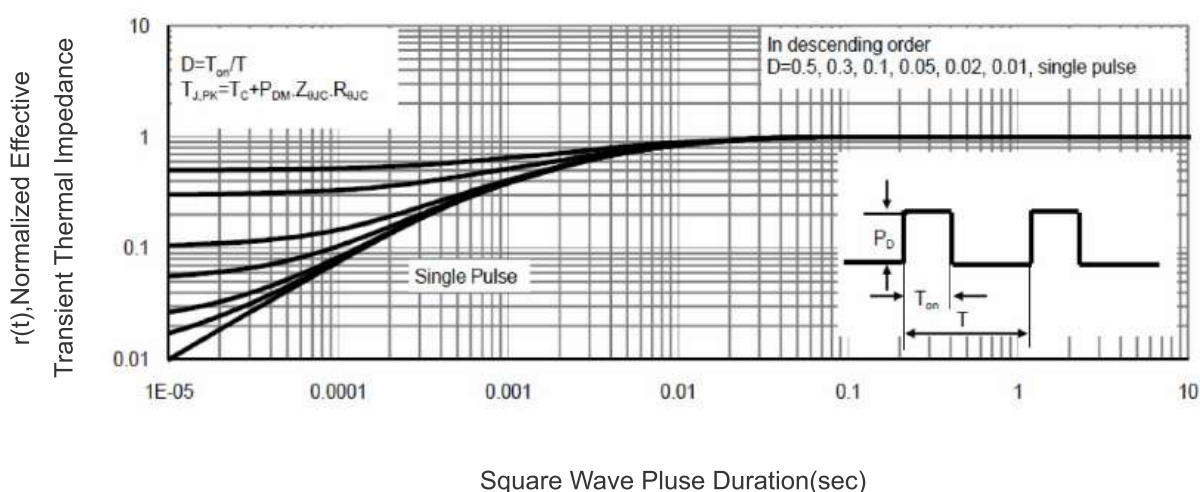
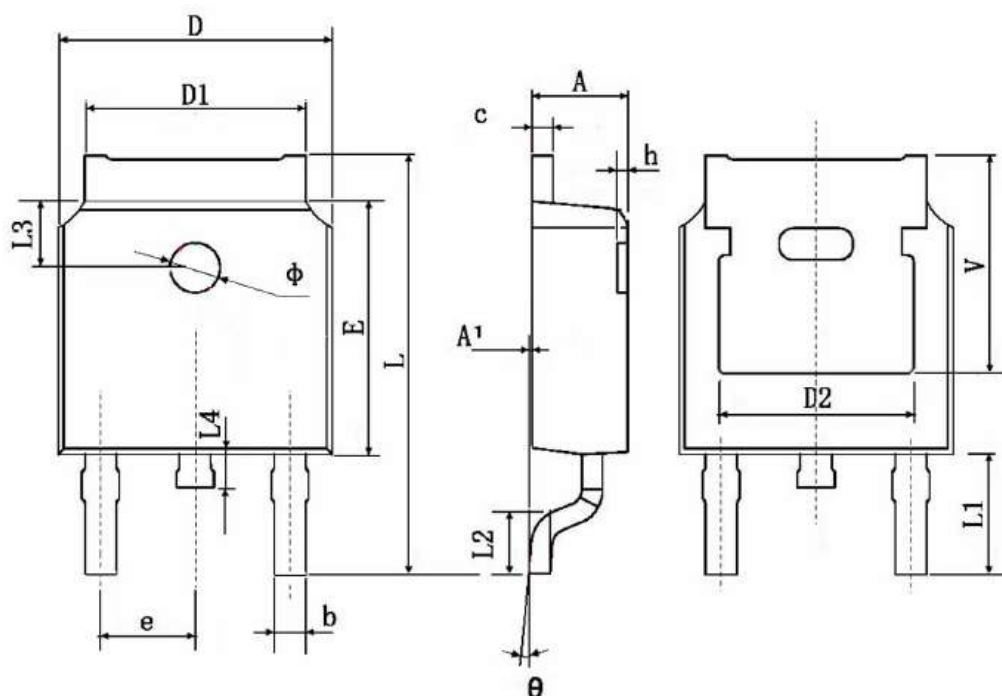


Figure 11 Normalized Maximum Transient Thermal Impedance

## TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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