

MJ N-Channel Enhancement Mode Power MOSFET

Description

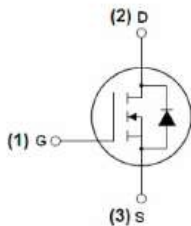
The MJ6075K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

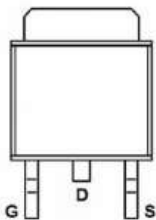
- ◆ $V_{DS} = 60V, I_D = 75A$
 $R_{DS(ON)} < 11.5m\Omega @ V_{GS} = 10V$ (Typ: 9.1m Ω)
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

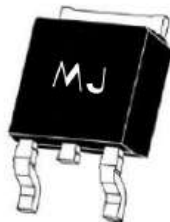
- ◆ Power switching application
- ◆ Hard switched and high frequency circuits
- ◆ Uninterruptible Power Supply



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ6075K	MJ6075K	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_c = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	75	A
Drain Current-Continuous($T_c = 100^{\circ}\text{C}$)	$I_{D(100^{\circ}\text{C})}$	50	A
Pulsed Drain Current	I_{DM}	300	A
Maximum Power Dissipation	P_D	110	W
Derating factor		0.73	W/ $^{\circ}\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	450	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.36	$^{\circ}\text{C/W}$
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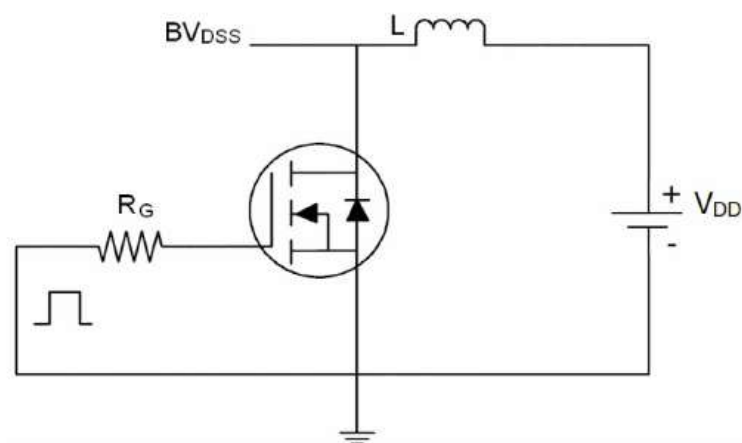
Electrical Characteristics (T_c =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	68	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	9.1	11.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V,I _D =30A	20	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V F=1.0MHz	-	2350	-	PF
Output Capacitance	C _{Oss}		-	237	-	PF
Reverse Transfer Capacitance	C _{rss}		-	205	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V,I _D =2A,R _L =15Ω V _{GS} =10V,R _{GEN} =2.5Ω	-	16	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}		-	45	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =30A V _{GS} =10V	-	50	-	nC
Gate-Source Charge	Q _{gs}		-	12	-	nC
Gate-Drain Charge	Q _{gd}		-	16	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =30A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	75	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =75A di/dt=100A/μs <small>(Note 3)</small>	-	28	-	nS
Reverse Recovery Charge	Q _{rr}		-	49	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

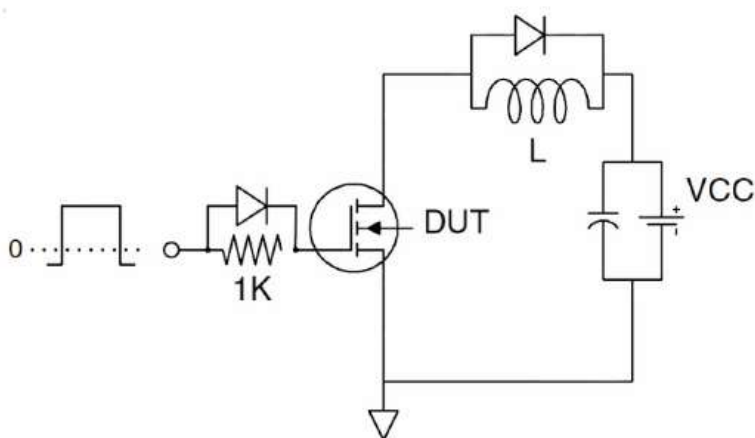
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C, V_{DD}=30V,V_G=10V,L=0.5mH,R_g=25Ω

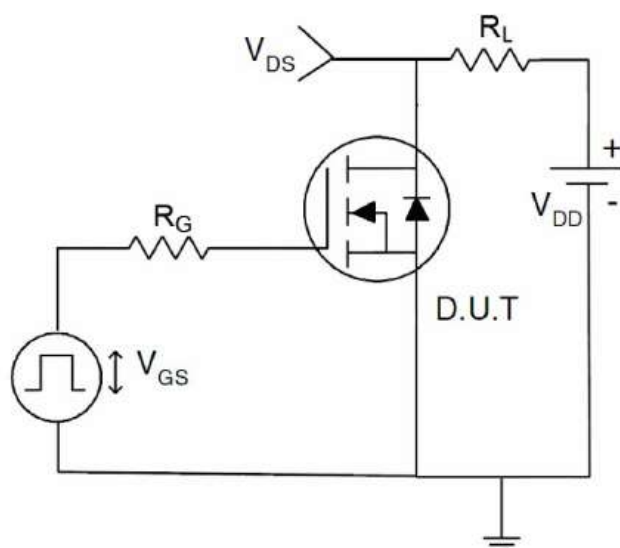
Test circuit



EAS test Circuit

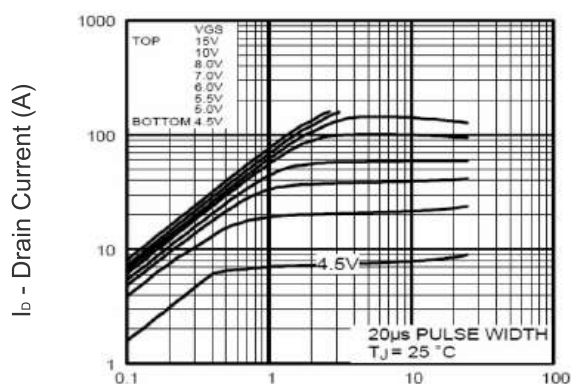


Gate charge test Circuit

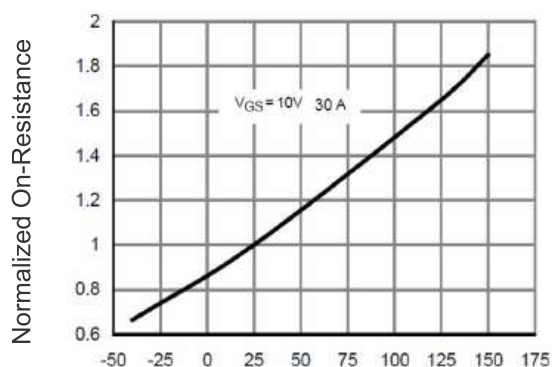


Switch Time Test Circuit

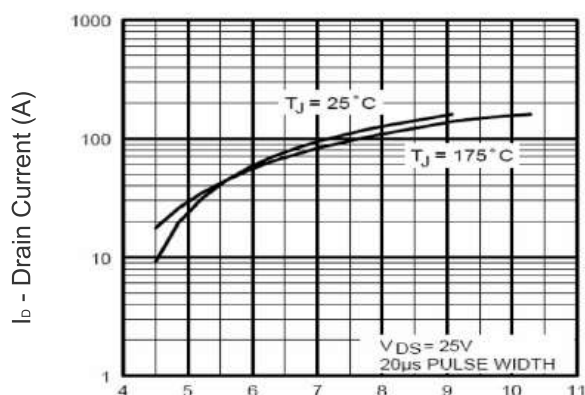
Typical Electrical and Thermal Characteristics (Curves)



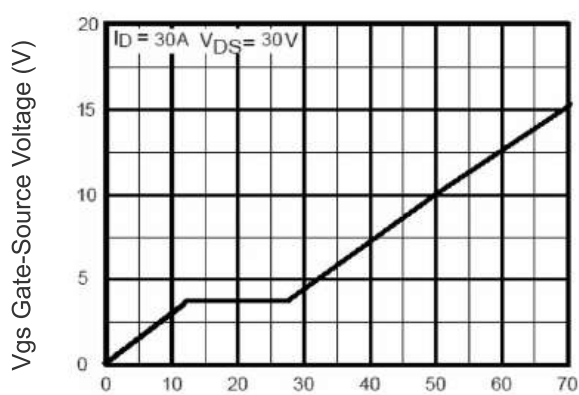
V_{DS} Drain-Source Voltage (V)
Figure 1 Output Characteristics



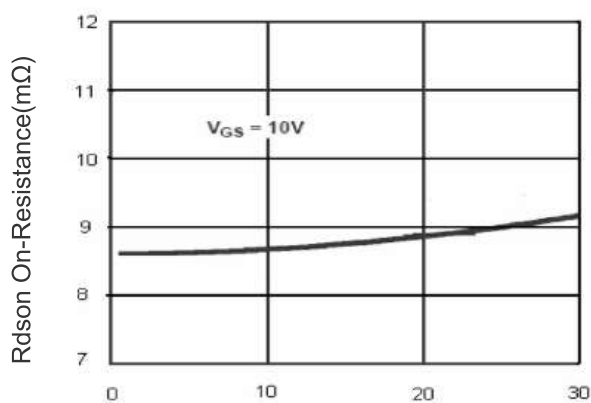
T_J -Junction Temperature($^\circ C$)
Figure 4 $R_{DS(on)}$ -Junction Temperature



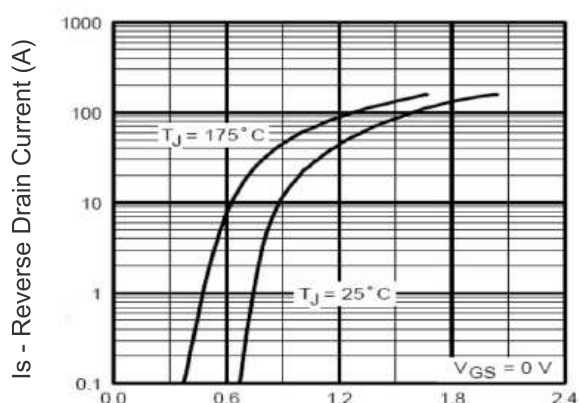
V_{GS} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



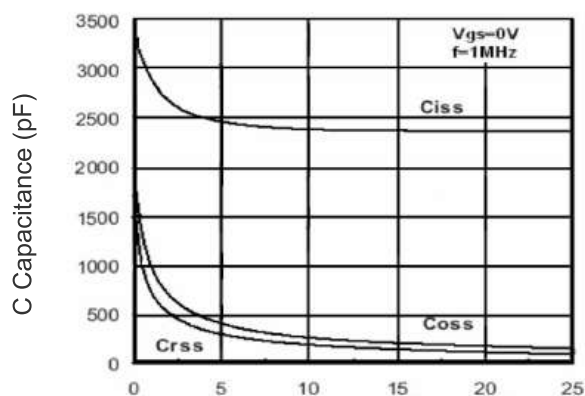
Q_g Gate Charge (nC)
Figure 5 Gate Charge



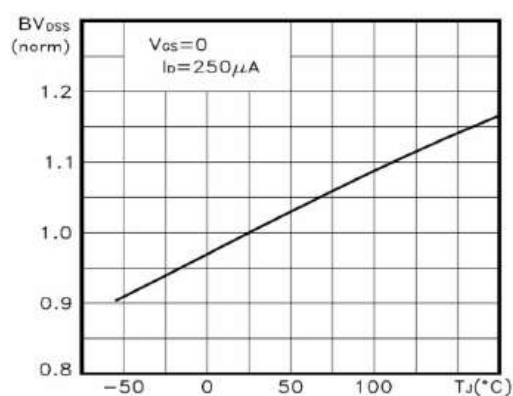
I_D - Drain Current (A)
Figure 3 $R_{DS(on)}$ - Drain Current



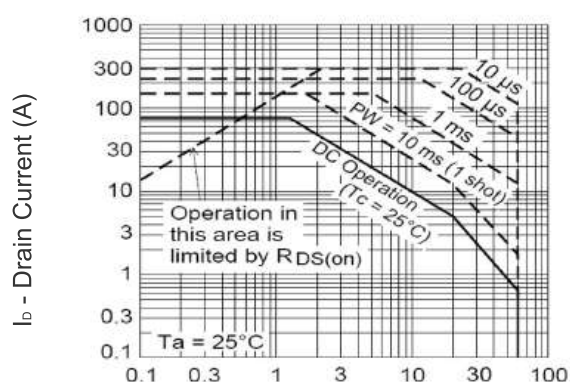
V_{SD} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



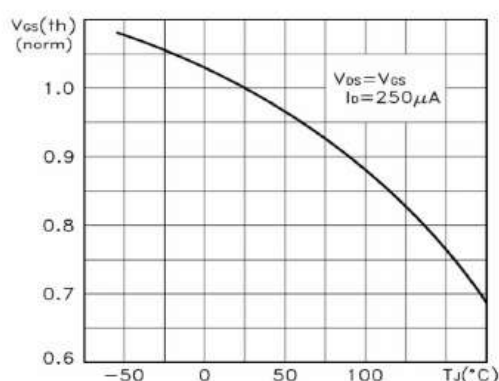
V_{ds} Drain-Source Voltage (V)
Figure 7 Capacitance vs V_{ds}



T_J -Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



V_{ds} Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J -Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature

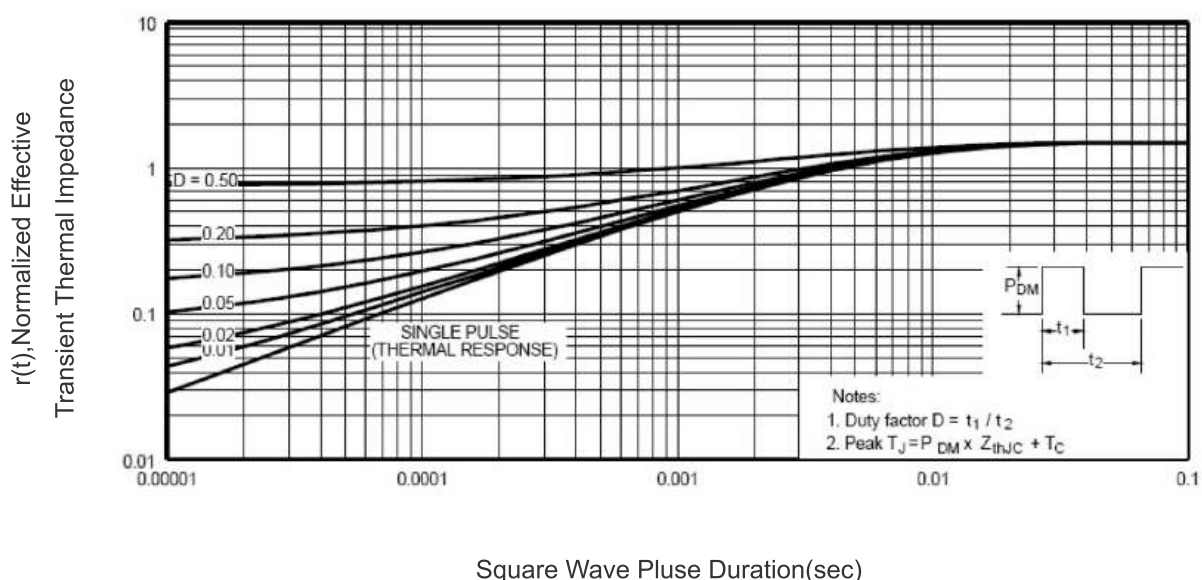
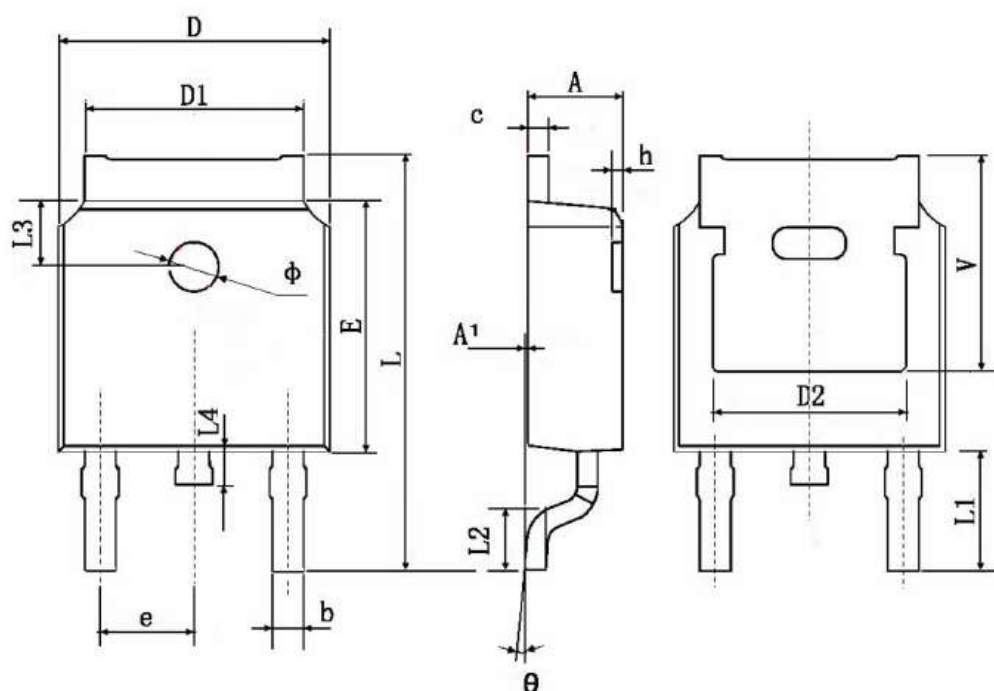


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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