

MJ N-Channel Enhancement Mode Power MOSFET

Description

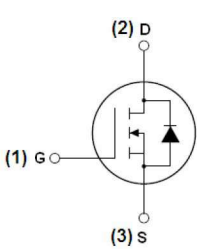
The MJ6020L uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

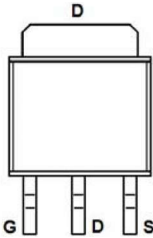
- ◆ $V_{DS} = 60V, I_D = 20A$
 $R_{DS(ON)} < 44m\Omega @ V_{GS} = 10V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

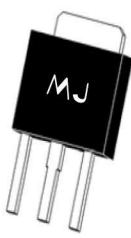
- ◆ Power management



Schematic diagram



Marking and pin assignment



TO-251S top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ6020L	MJ6020L	TO-251S	-	-	-

Absolute Maximum Ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous($T_c = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	14	A
Pulsed Drain Current	I_{DM}	45	A
Maximum Power Dissipation	P_D	30	W
Derating factor		0.2	W/ $^{\circ}C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	72	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	5	$^{\circ}C/W$
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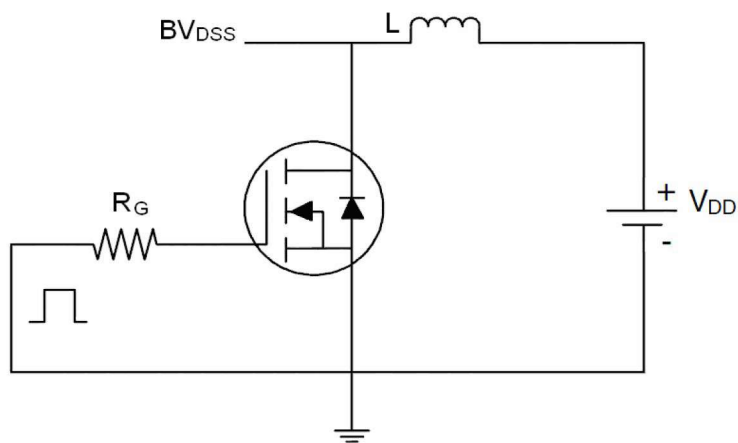
Electrical Characteristics (Tc =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.0	2.0	3.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	37	44	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =4.5A	11	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V F=1.0MHz	-	500	-	PF
Output Capacitance	C _{oss}		-	60	-	PF
Reverse Transfer Capacitance	C _{rss}		-	25	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V,I _D =2A,R _L =6.7Ω V _{GS} =10V,R _G =3Ω	-	5	-	nS
Turn-on Rise Time	t _r		-	2.6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	16.1	-	nS
Turn-Off Fall Time	t _f		-	2.3	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =4.5A V _{GS} =10V	-	14	-	nC
Gate-Source Charge	Q _{gs}		-	2.9	-	nC
Gate-Drain Charge	Q _{gd}		-	5.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	20	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =20A di/dt=100A/μs ^(Note 3)	-	35	-	nS
Reverse Recovery Charge	Q _{rr}		-	53	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

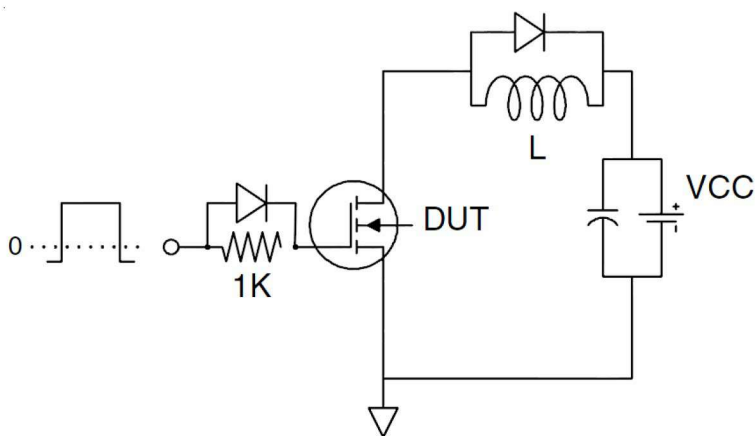
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition:T_J=25℃,V_{DD}=30V,V_G=10V,L=0.1mH,R_g=25Ω

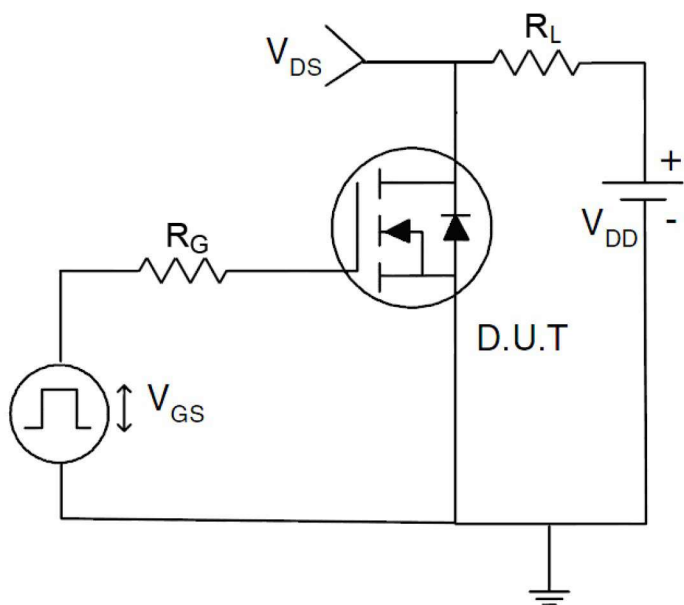
Test circuit



EAS test Circuit

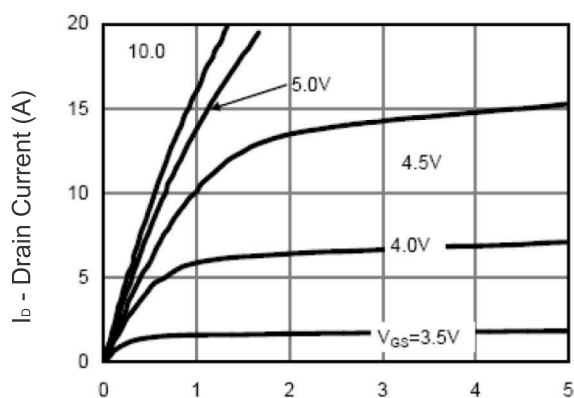


Gate charge test Circuit

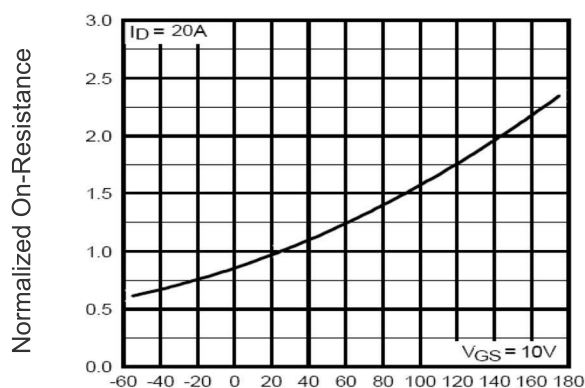


Switch Time Test Circuit

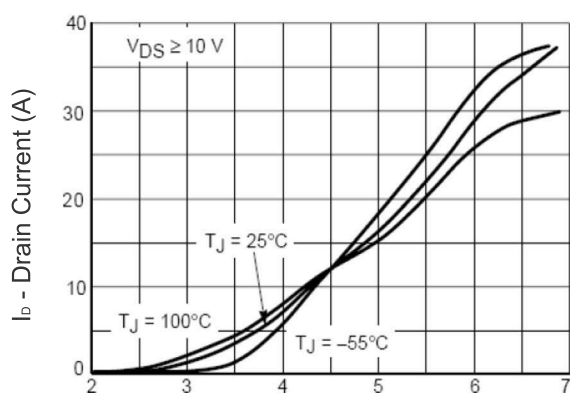
Typical Electrical and Thermal Characteristics (Curves)



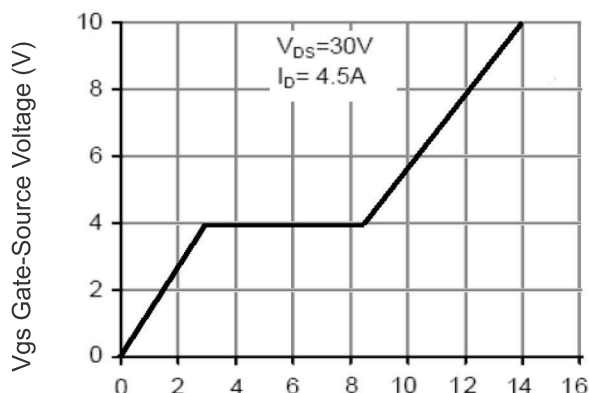
V_{DS} Drain-Source Voltage (V)
Figure 1 Output Characteristics



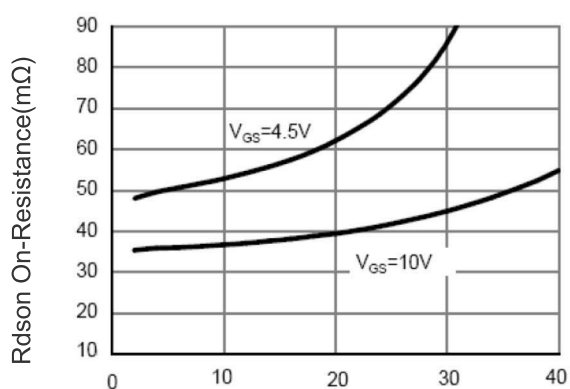
T_J -Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



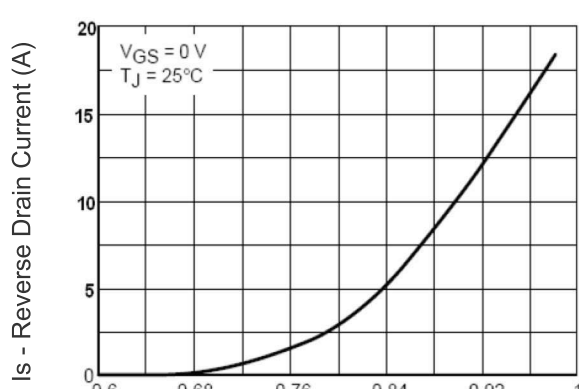
V_{GS} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



Q_g Gate Charge (nC)
Figure 5 Gate Charge



I_D - Drain Current (A)
Figure 3 Rdson- Drain Current



V_{SD} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward

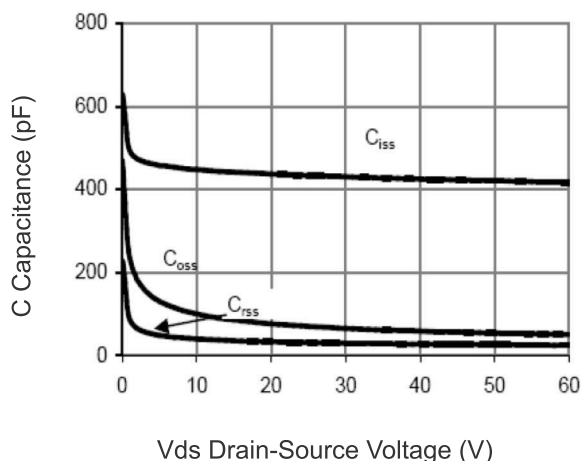


Figure 7 Capacitance vs Vds

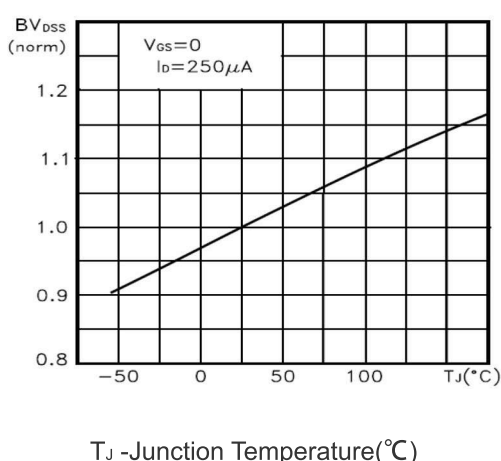


Figure 9 BV_{DSS} vs Junction Temperature

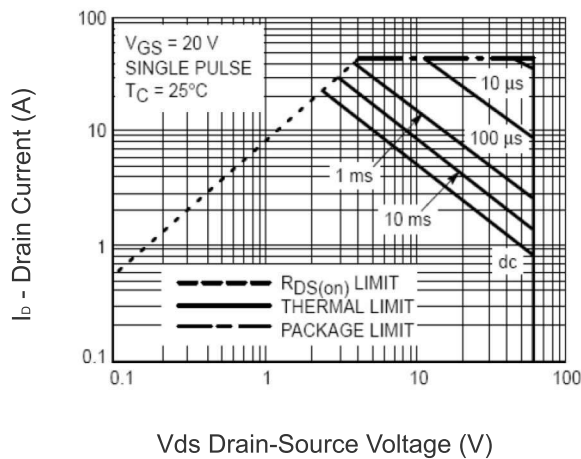


Figure 8 Safe Operation Area

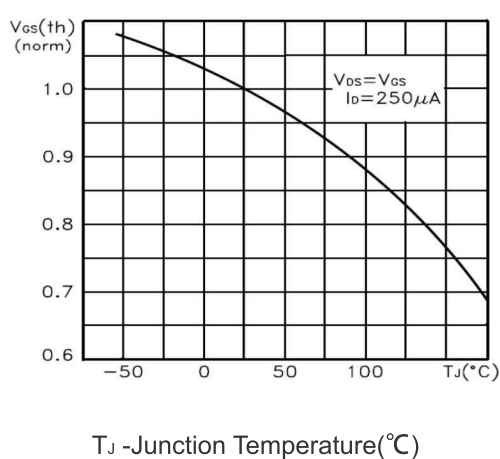


Figure 10 V_{GS(th)} vs Junction Temperature

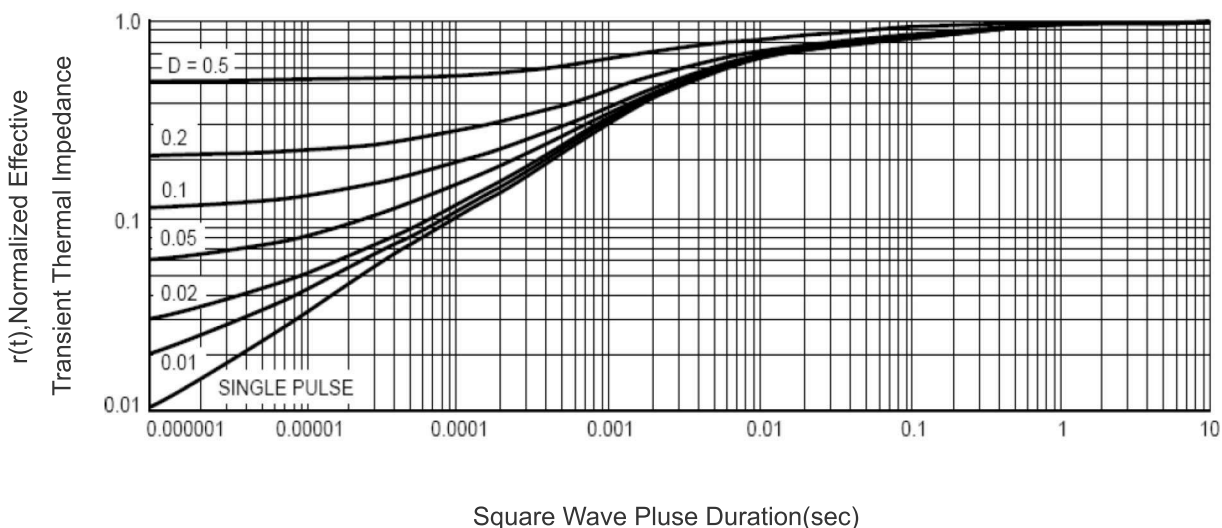
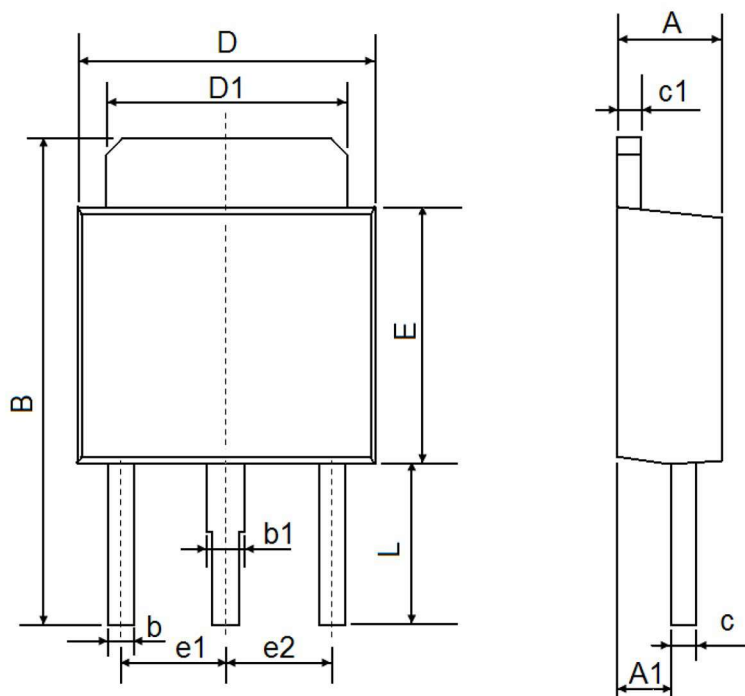


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-251S Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.250	2.350	0.089	0.093
A1	1.150	1.250	0.045	0.049
B	10.200	10.800	0.402	0.425
b	0.550	0.650	0.022	0.026
b1	0.750	0.850	0.030	0.033
c	0.480	0.540	0.019	0.021
c1	0.480	0.540	0.019	0.021
D	6.400	6.600	0.252	0.260
D1	5.250	5.350	0.207	0.211
E	5.400	5.600	0.213	0.220
e1	2.300 TYP		0.091 TYP	
e2	2.300 TYP		0.091 TYP	
L	3.300	3.700	0.130	0.146

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