MJ N-Channel Enhancement Mode Power MOSFET

Description

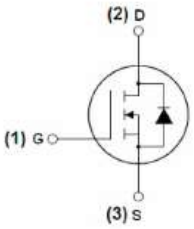
The MJ6020AK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

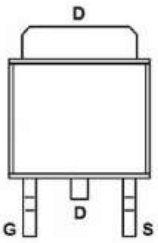
- V_{DS} =60V,I_D =20A
  $R_{DS(ON)}$ <35mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <40mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

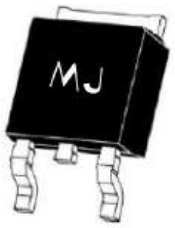
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ6020AK	MJ6020AK	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous(T_C =100℃)	$I_{D(100℃)}$	14	A
Pulsed Drain Current (Note 1)	I_{DM}	60	A
Maximum Power Dissipation	P_D	45	W
Derating factor		0.3	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	72	mJ
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	3.3	℃/W

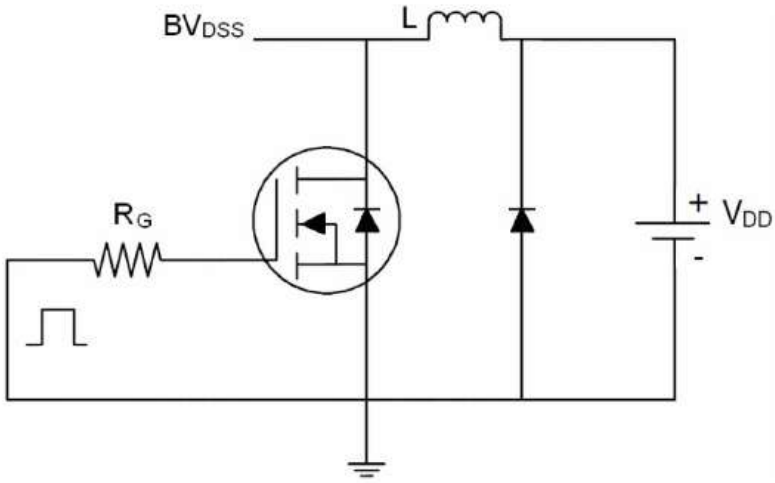
Electrical Characteristics (T_C =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=250μA	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	-	24	35	mΩ
		V_{GS}=4.5V, I_D=10A	-	30	40	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=10A	11	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V F=1.0MHz	-	973.2	-	PF
Output Capacitance	C_{oss}		-	61.2	-	PF
Reverse Transfer Capacitance	C_{rss}		-	58.8	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, R_L=3Ω V_{GS}=10V,R_G=3Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	16	-	nS
Turn-Off Fall Time	t_f		-	23	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=10A V_{GS}=10V	-	25	-	nC
Gate-Source Charge	Q_{gs}		-	4.5	-	nC
Gate-Drain Charge	Q_{gd}		-	6.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=10A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	20	A
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=10A di/dt=100A/μs (Note 3)	-	29	-	nS
Reverse Recovery Charge	Q_{rr}		-	49	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

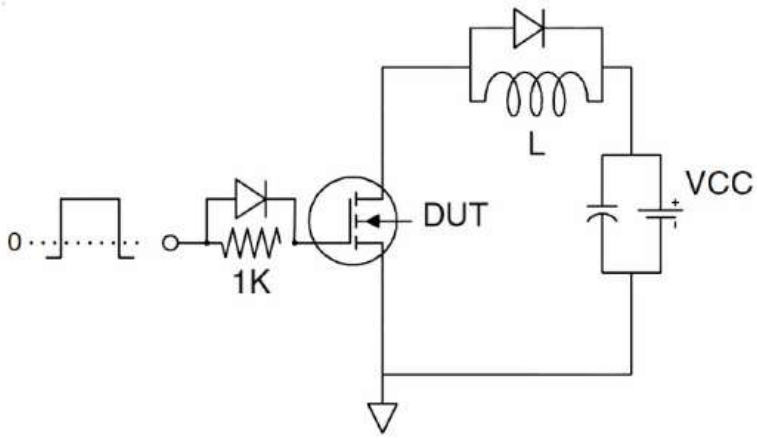
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition: Tj=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

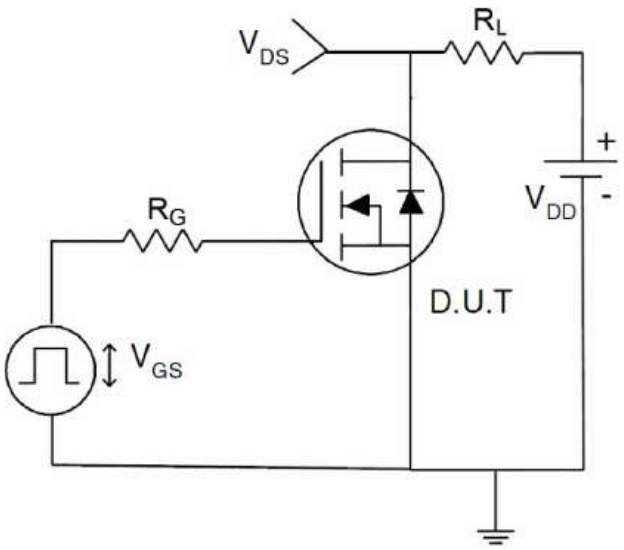
Test circuit



EAS test Circuit

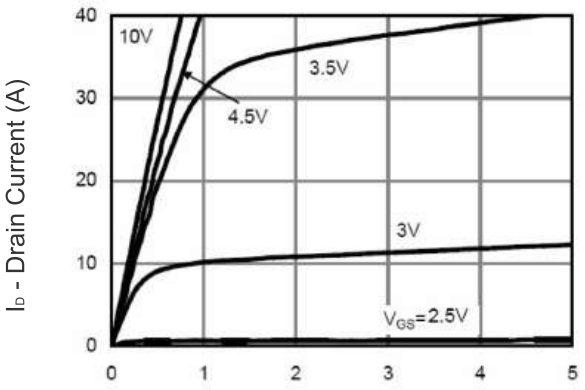


Gate charge test Circuit



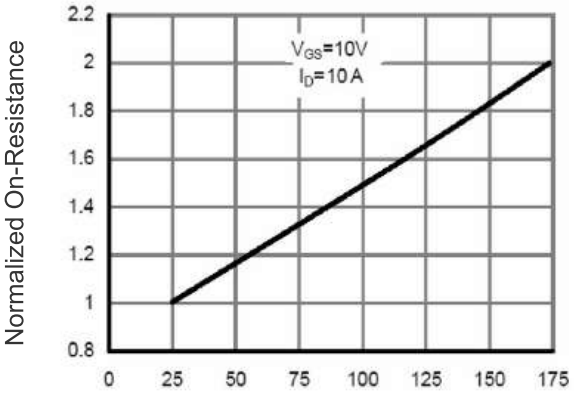
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



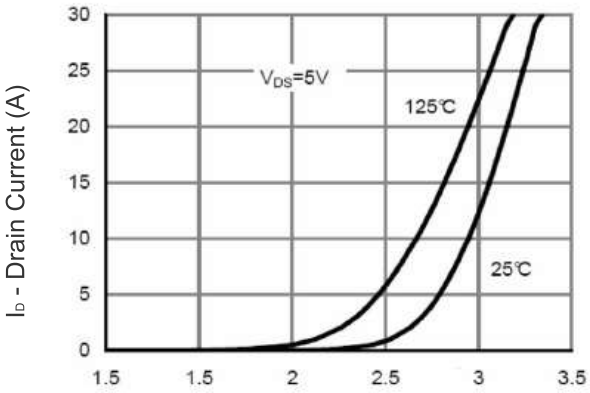
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



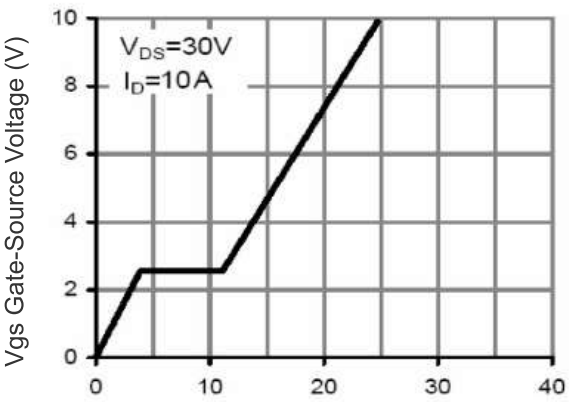
TJ -Junction Temperature(℃)

Figure 4 Rdson-Junction Temperature



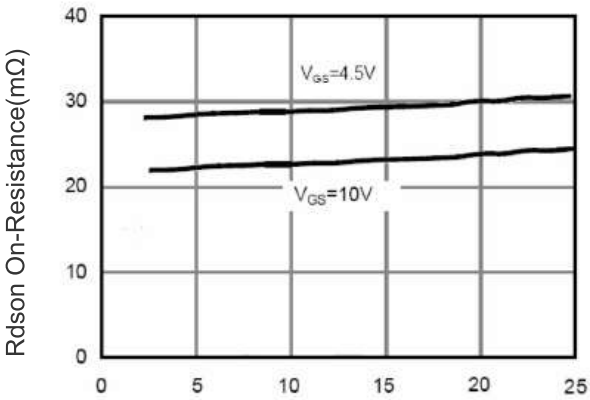
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



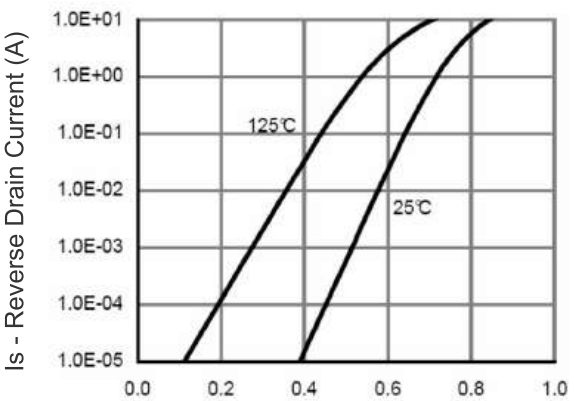
Qg Gate Charge (nC)

Figure 5 Gate Charge



ID - Drain Current (A)

Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

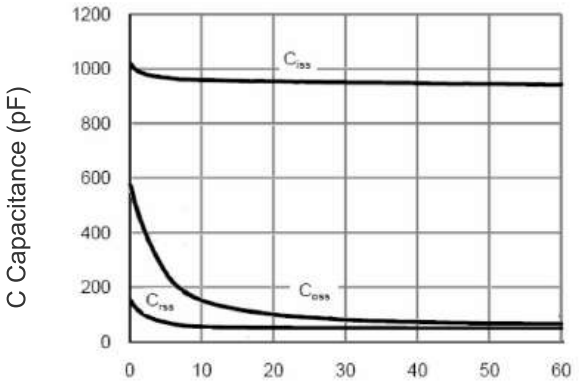


Figure 7 Capacitance vs Vds

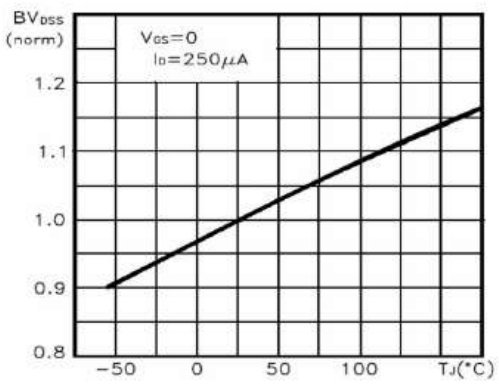


Figure 9 BV_{DSS} vs Junction Temperature

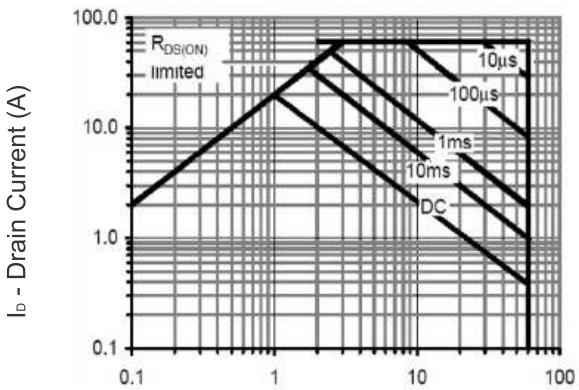


Figure 8 Safe Operation Area

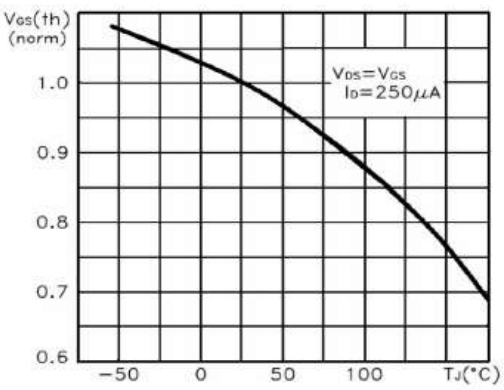


Figure 10 $V_{GS(th)}$ vs Junction Temperature

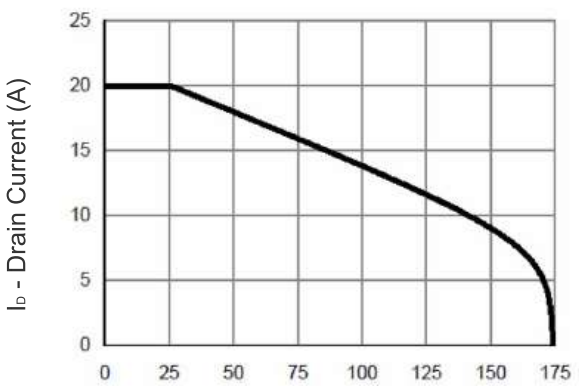


Figure 11 Current De-rating

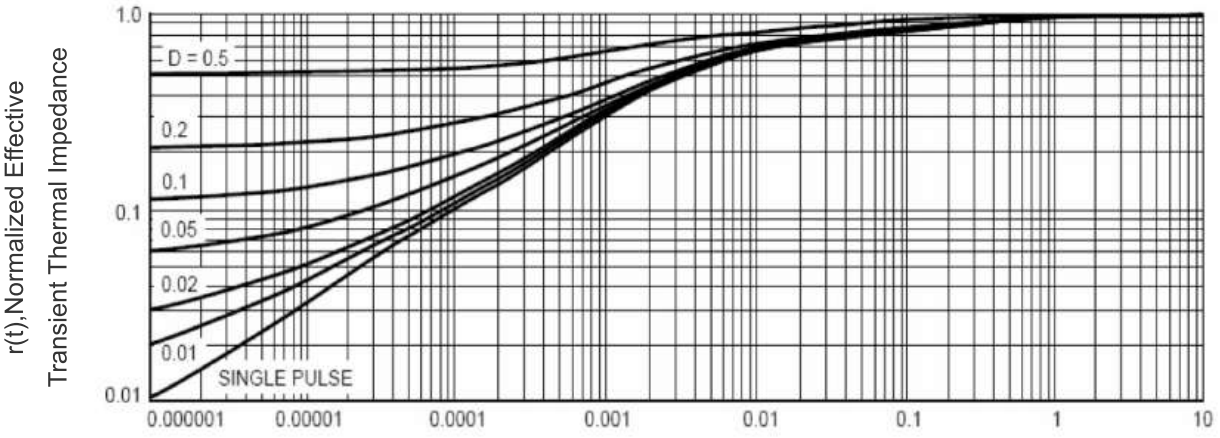
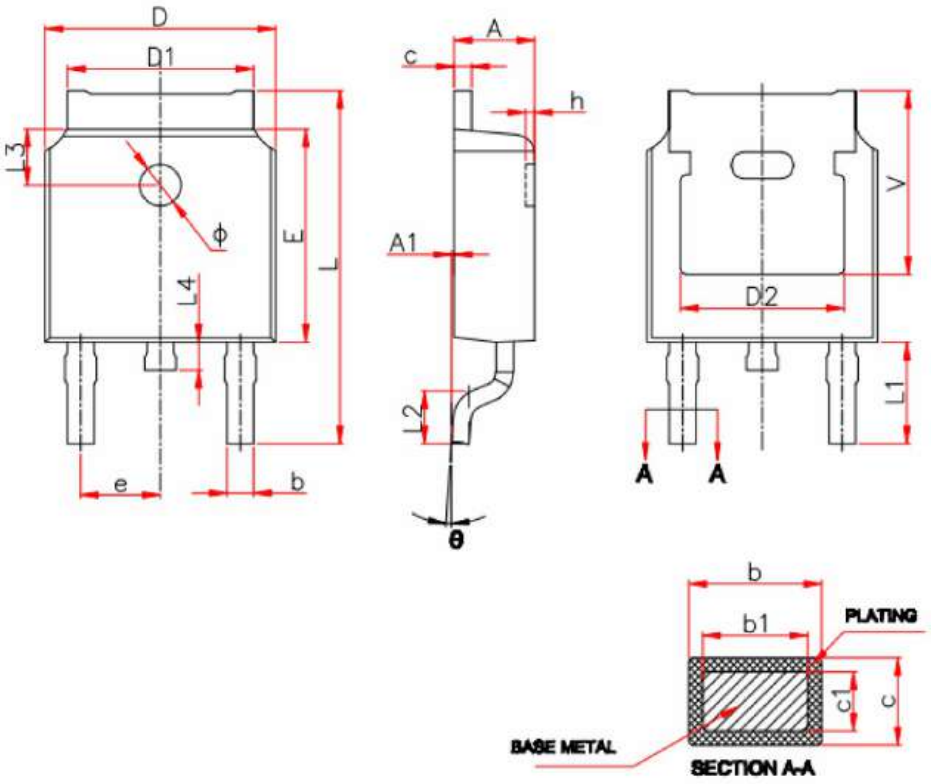


Figure 12 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
Φ	1.10	1.30
θ	0°	8°

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