

MJ N-Channel Enhancement Mode Power MOSFET

Description

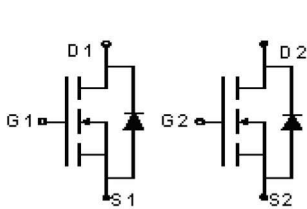
The MJ6005S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

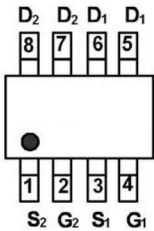
- ◆ $V_{DS} = 60V, I_D = 4.5A$
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = 10V$ (Typ: $38m\Omega$)
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Low gate to drain charge to reduce switching losses

Application

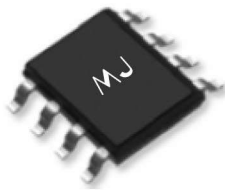
- ◆ Power switching application
- ◆ Hard switched and high frequency circuits
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



SOP-8 top view

100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
6005	MJ6005S	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	4.5	A
Drain Current-Continuous($T_C = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	3.0	A
Pulsed Drain Current	I_{DM}	20	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	$^{\circ}C/W$
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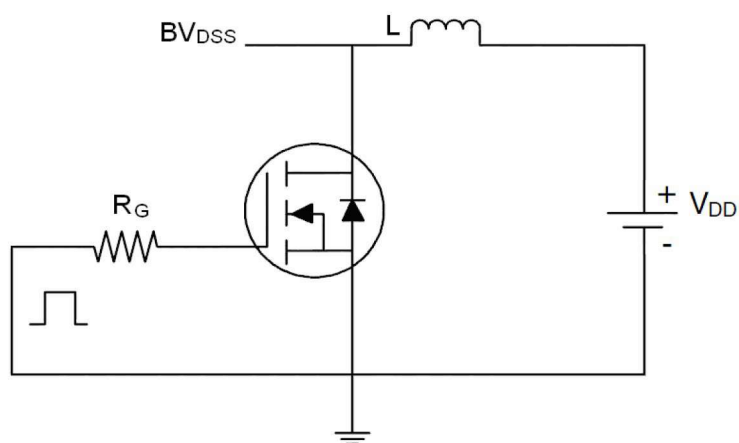
Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V,I _D =250μA	60	69	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =4.5A	-	38	45	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =4.5A	11	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V F=1.0MHz	-	450	-	PF
Output Capacitance	C _{oss}		-	60	-	PF
Reverse Transfer Capacitance	C _{rss}		-	25	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DS} =30V,I _D =4.5A V _{GS} =10V,R _{GEN} =3Ω	-	4.7	-	nS
Turn-on Rise Time	t _r		-	2.3	-	nS
Turn-Off Delay Time	t _{d(off)}		-	15.7	-	nS
Turn-Off Fall Time	t _f		-	1.9	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =4.5A V _{GS} =10V	-	8.5	-	nC
Gate-Source Charge	Q _{gs}		-	1.6	-	nC
Gate-Drain Charge	Q _{gd}		-	2.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =4.5A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	4.5	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =4.5A di/dt= 100A/μs ^(Note 3)	-	25	-	nS
Reverse Recovery Charge	Q _{rr}		-	35	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

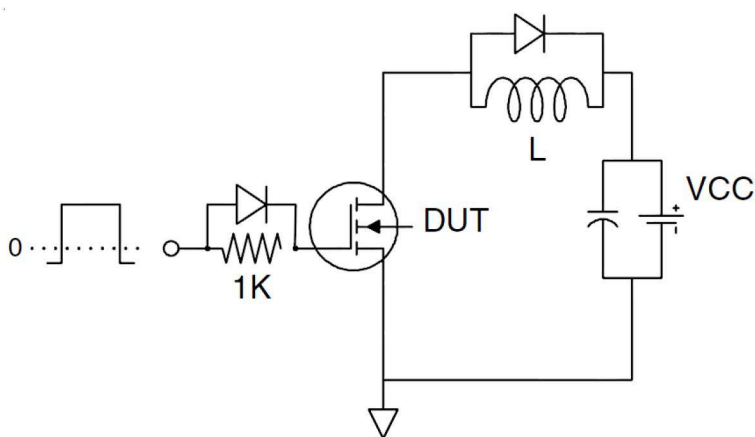
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production

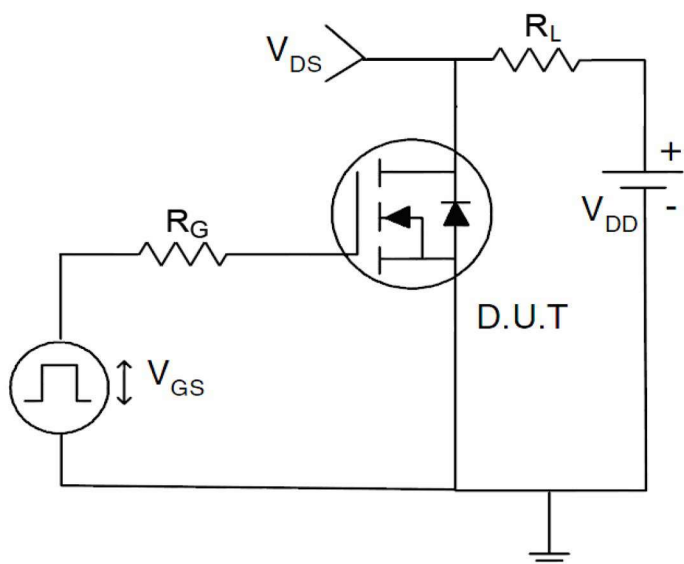
Test circuit



EAS test Circuit

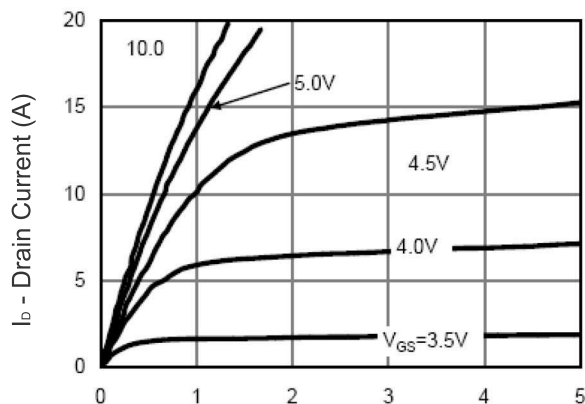


Gate charge test Circuit

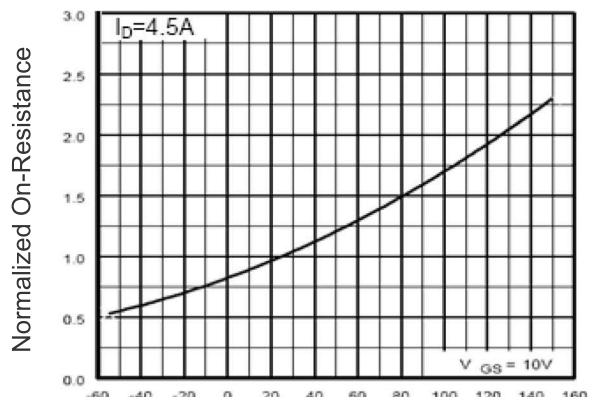


Switch Time Test Circuit

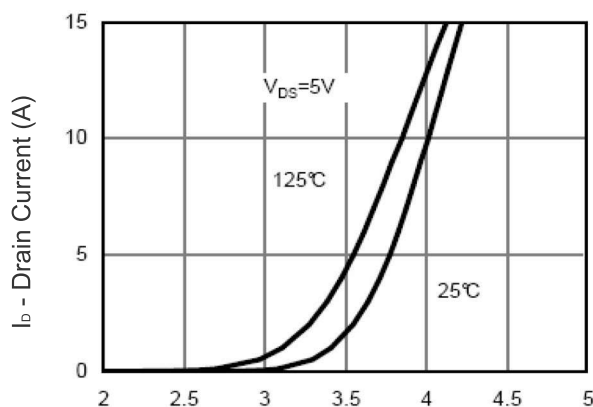
Typical Electrical and Thermal Characteristics (Curves)



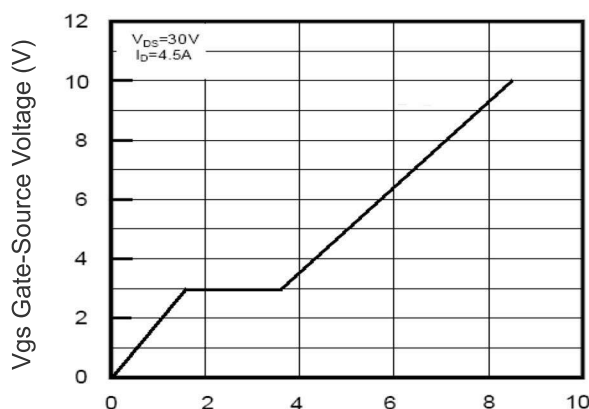
V_{ds} Drain-Source Voltage (V)
Figure 1 Output Characteristics



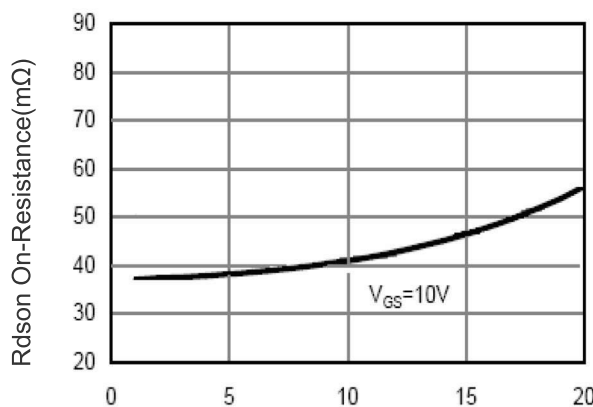
T_J -Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



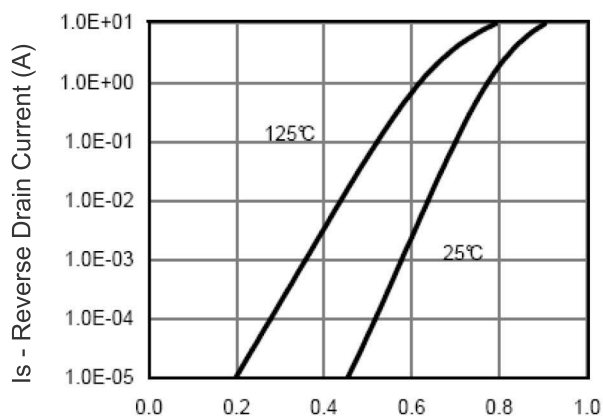
V_{gs} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



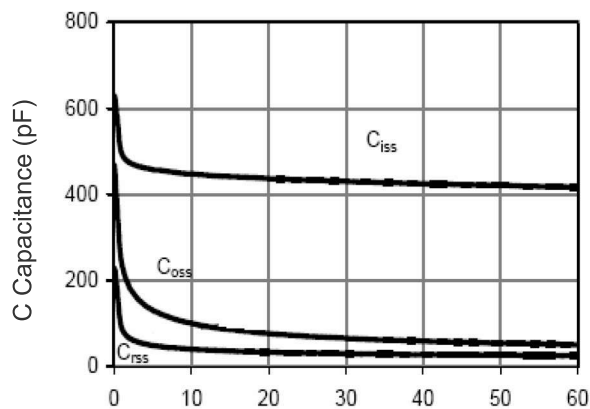
Q_g Gate Charge (nC)
Figure 5 Gate Charge



I_D - Drain Current (A)
Figure 3 Rdson- Drain Current

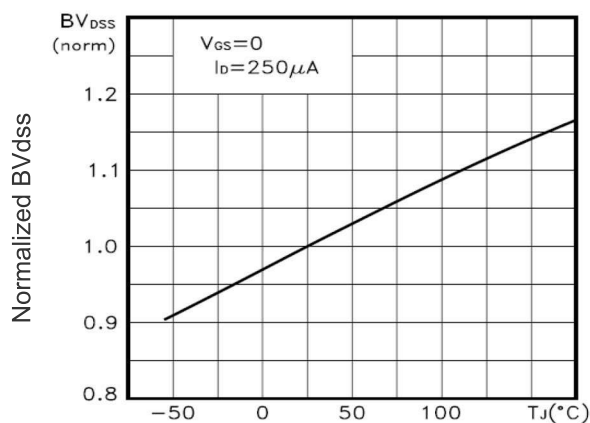


V_{sd} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



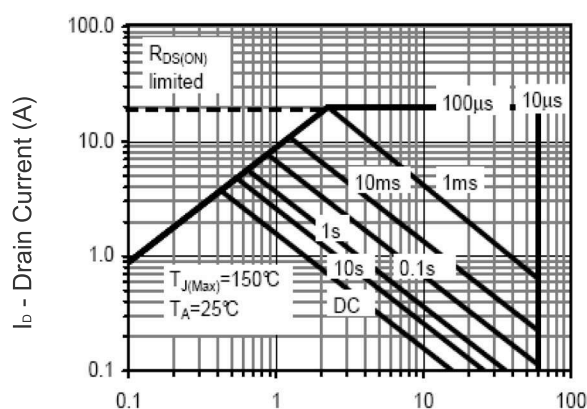
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



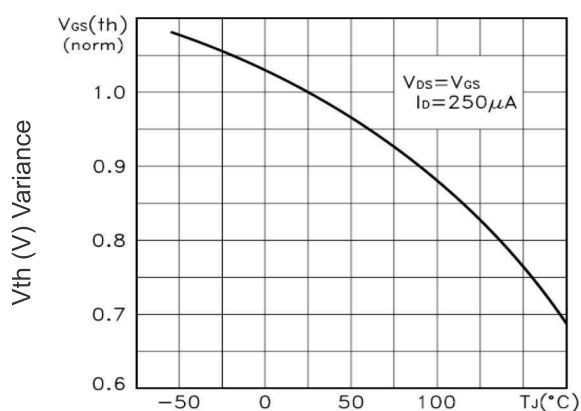
TJ -Junction Temperature(°C)

Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ -Junction Temperature(°C)

Figure 10 V_{GS(th)} vs Junction Temperature

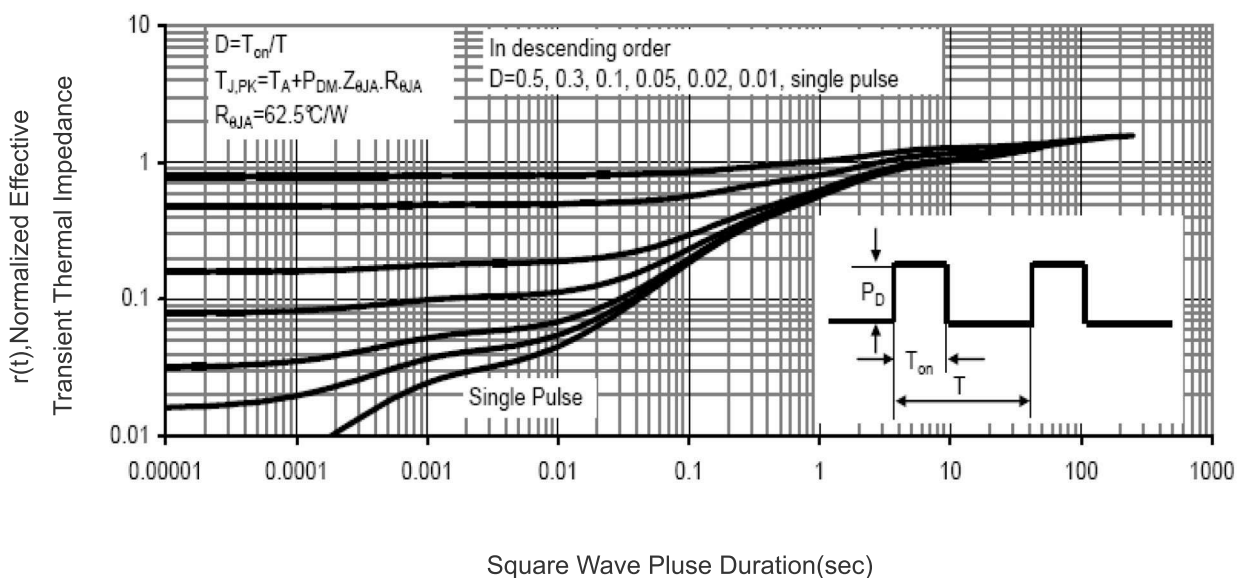
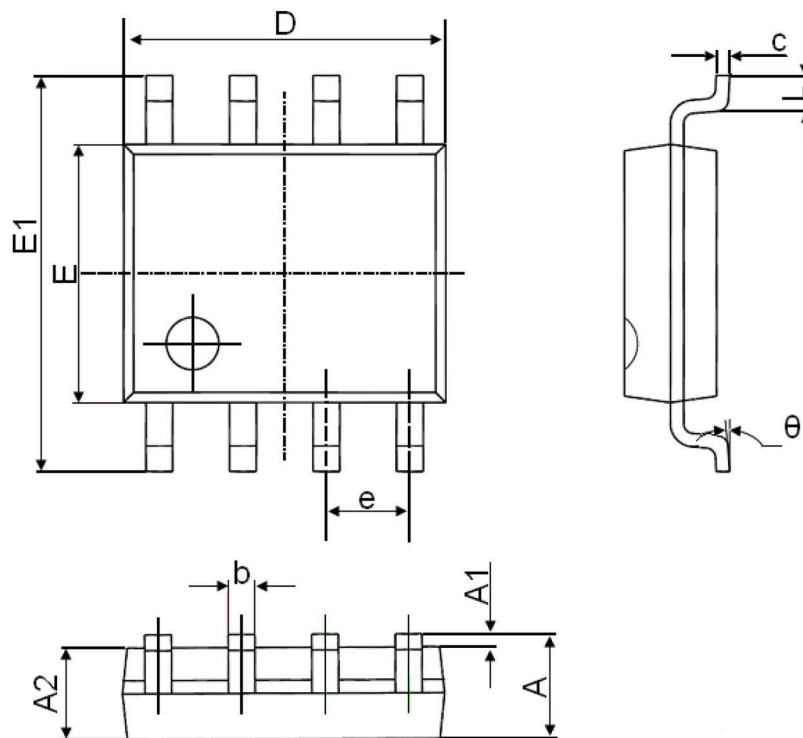


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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