

# MJ N-Channel Enhancement Mode Power MOSFET

## Description

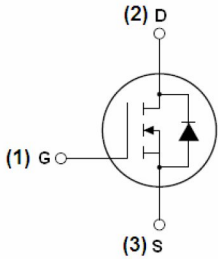
The MJ5520Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

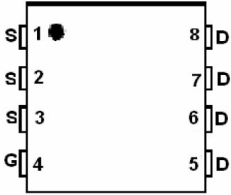
- ◆  $V_{DS}=55V, I_D=20A$   
 $R_{DS(ON)}<22m\Omega$  @  $V_{GS}=10V$  (Typ:19m $\Omega$ )
- ◆ High density cell design for ultra low  $R_{dson}$
- ◆ Fully characterized avalanche voltage and current

## Application

- ◆ Industrial power supplies
- ◆ LED backlighting



Schematic Diagram



Pin assignment



DFN3X3 EP top view

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ5520Q	MJ5520Q	DFN3X3EP	-	-	-

## Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	55	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous (Note 1)	$I_D$	20	A
Drain Current-Continuous( $T_C =100^{\circ}C$ )	$I_{D(100^{\circ}C)}$	14	A
Pulsed Drain Current	$I_{DM}$	60	A
Maximum Power Dissipation	$P_D$	35	W
Derating factor		0.23	W/°C
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

## Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JA}$	3.6	°C/W
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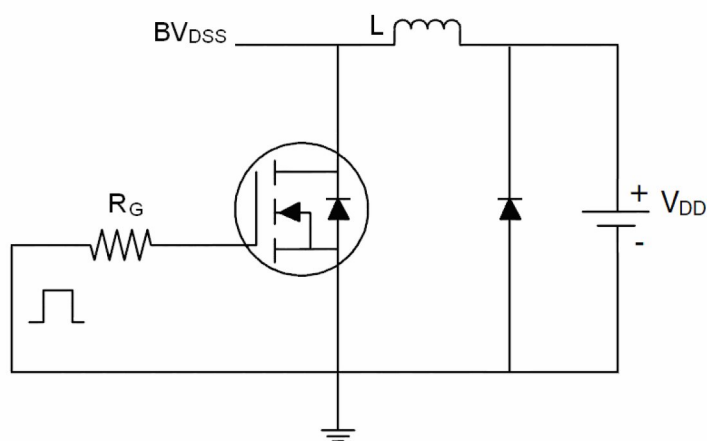
Electrical Characteristics (T<sub>A</sub> =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	55	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =55V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	2	3	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	19	22	mΩ
Dynamic Characteristics <sup>(Note 4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V,V <sub>GS</sub> =0V, F=1.0MHz	-	1340	-	PF
Output Capacitance	C <sub>oss</sub>		-	123	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	10	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =25V,I <sub>D</sub> =2A R <sub>L</sub> =3Ω,R <sub>G</sub> =3Ω	-	6	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	2.5	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	22	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	2.5	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =25V,I <sub>D</sub> =10A, V <sub>GS</sub> =10V	-	21	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	20	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> =25°C, I <sub>F</sub> =10A di/dt=100A/μs <sup>(Note 3)</sup>	-	16		nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	38		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

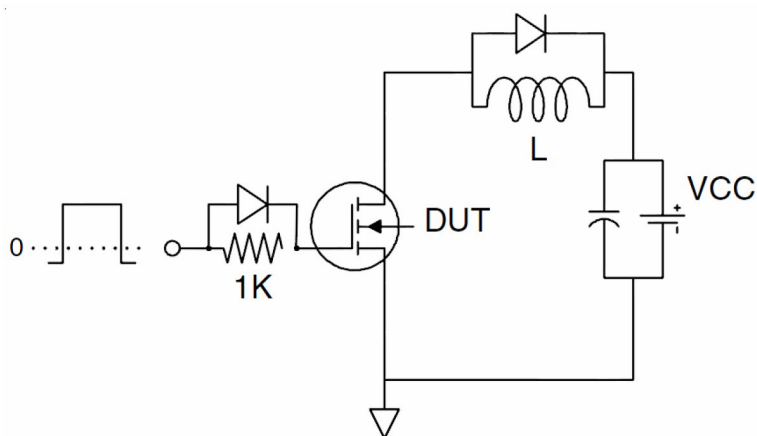
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T<sub>J</sub>=25℃, V<sub>DD</sub>=15V,V<sub>G</sub>=10V,L=0.5mH,R<sub>G</sub>=25Ω

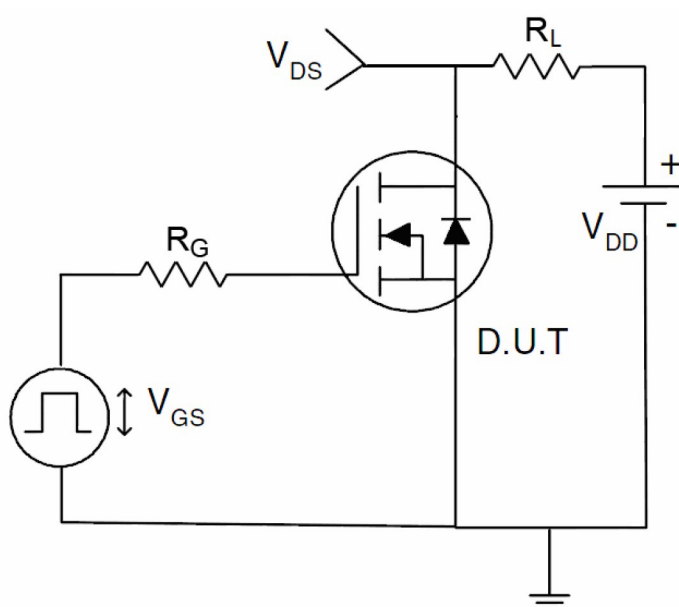
# Test circuit



EAS test Circuit

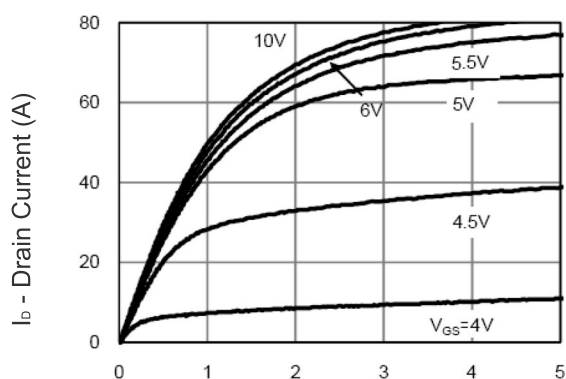


Gate charge test Circuit



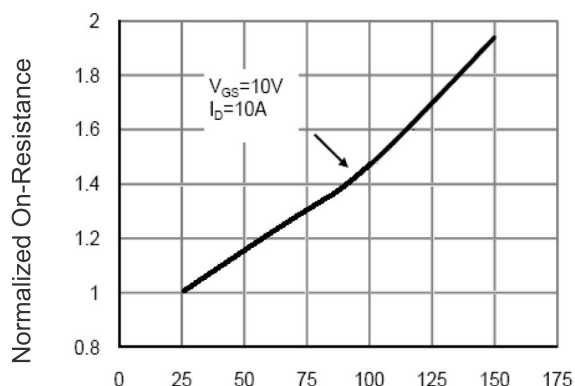
Switch Time Test Circuit

## Typical Electrical and Thermal Characteristics (Curves)



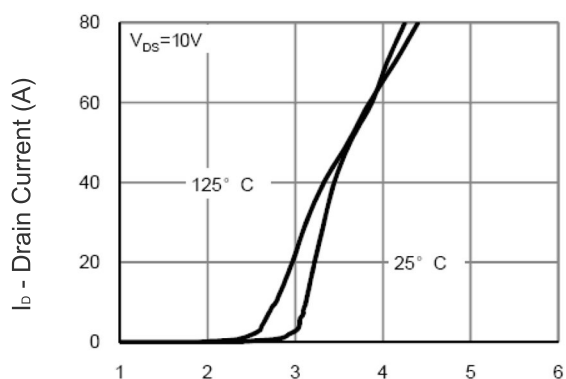
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



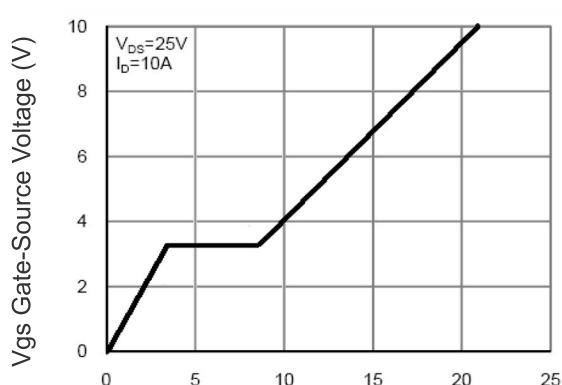
Tj -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



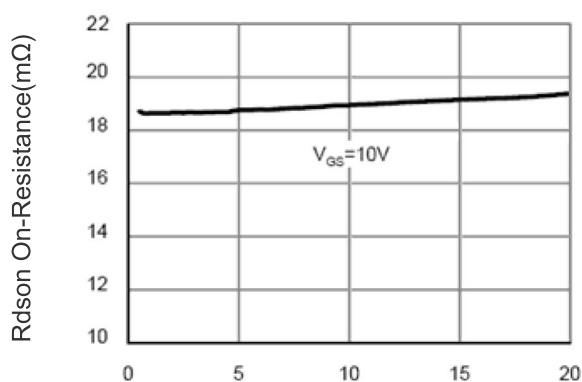
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



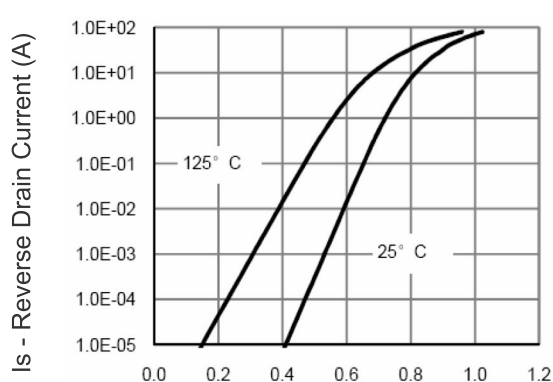
Qg Gate Charge (nC)

Figure 5 Gate Charge



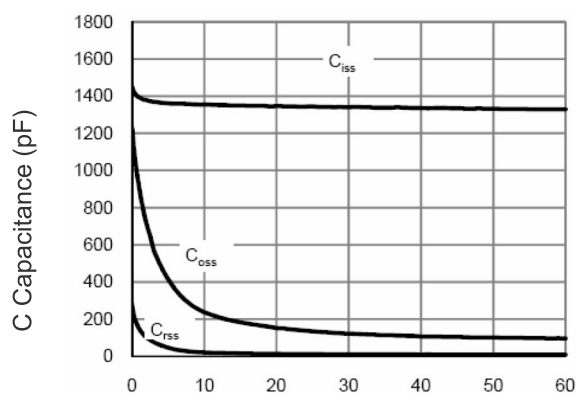
Id - Drain Current (A)

Figure 3 Rdson- Drain Current

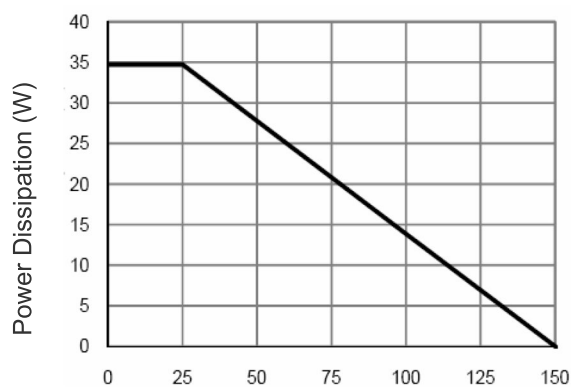


Vsd Source-Drain Voltage (V)

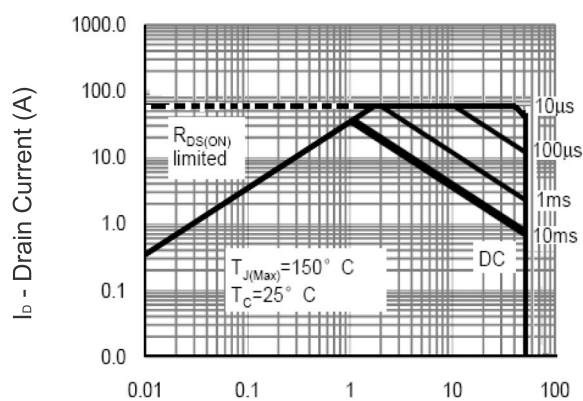
Figure 6 Source- Drain Diode Forward



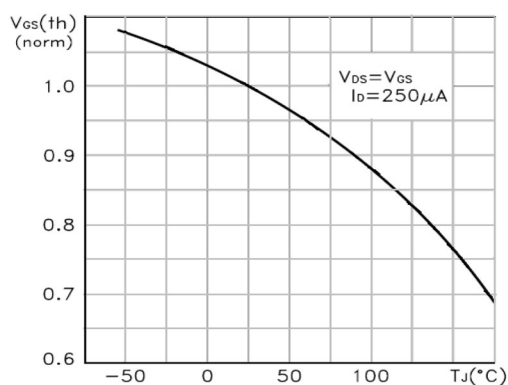
Vds Drain-Source Voltage (V)  
Figure 7 Capacitance vs Vds



T<sub>J</sub> -Junction Temperature(°C)  
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)  
Figure 8 Safe Operation Area



T<sub>J</sub> -Junction Temperature(°C)  
Figure 10 V<sub>GS(th)</sub> vs Junction Temperature

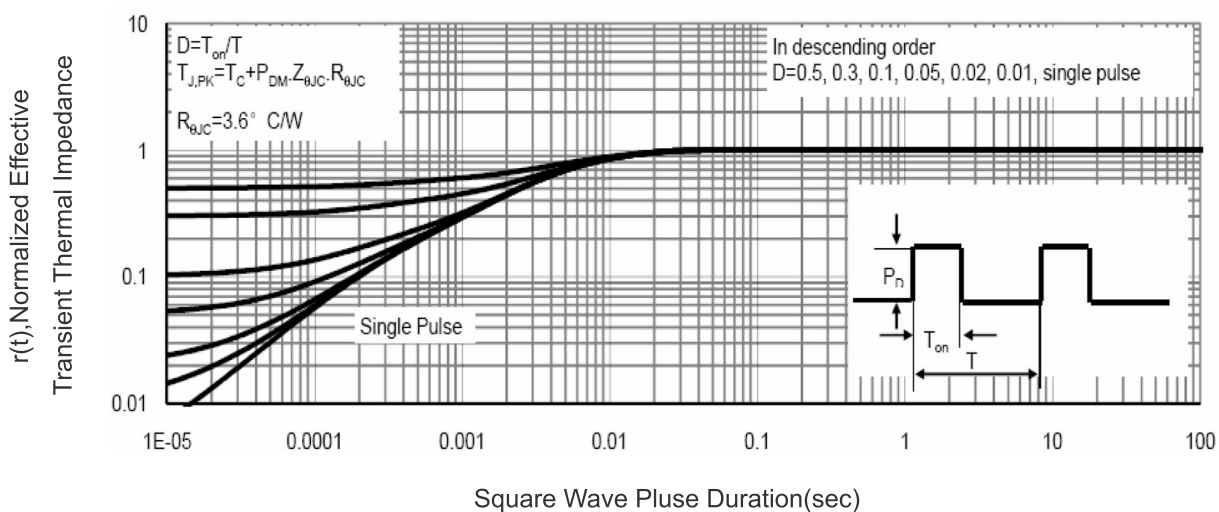
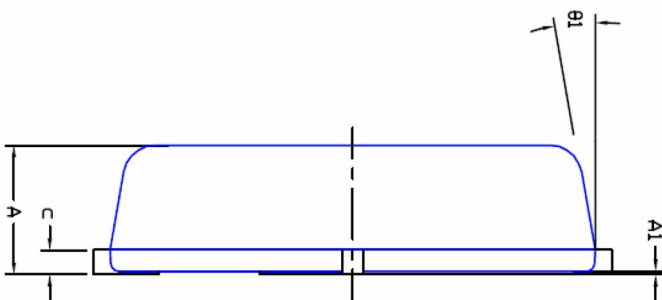
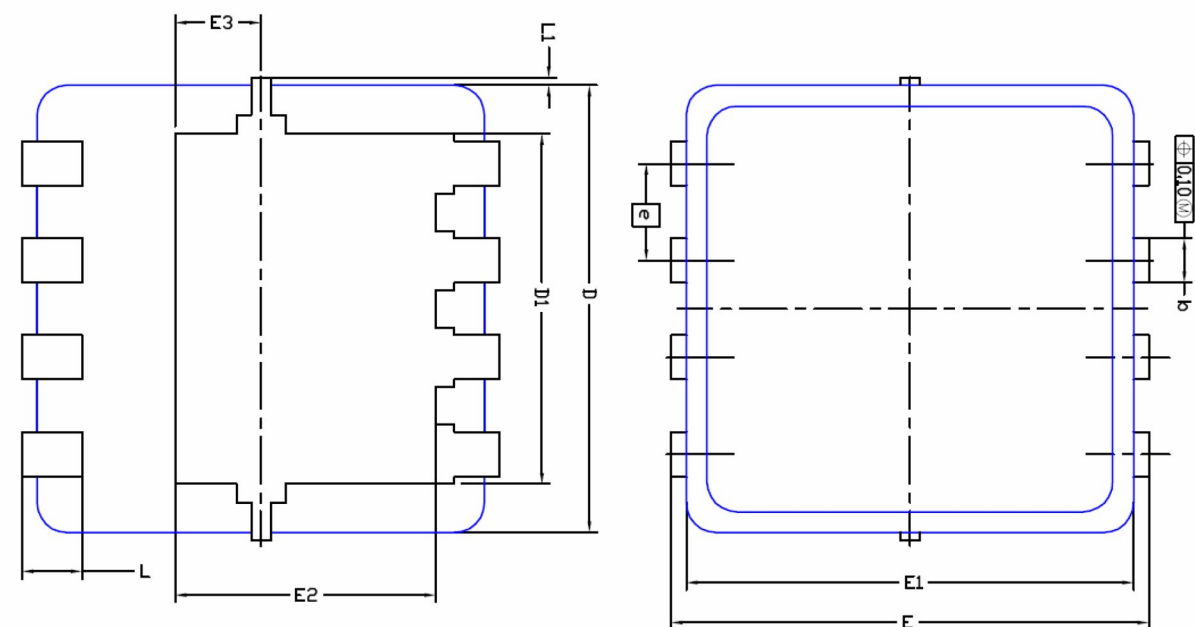


Figure 11 Normalized Maximum Transient Thermal Impedance

### DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°

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