

MJ N-Channel Enhancement Mode Power MOSFET

Description

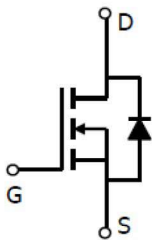
The MJ5015S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

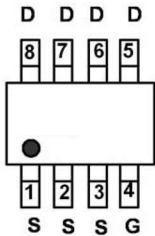
- ◆ $V_{DS} = 60V, I_D = 12A$
 $R_{DS(ON)} < 7.6m\Omega @ V_{GS} = 10V$ (Typ: 5.7m Ω)
 $R_{DS(ON)} < 8.0m\Omega @ V_{GS} = 4.5V$ (Typ: 6.3m Ω)
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Low gate to drain charge to reduce switching losses

Application

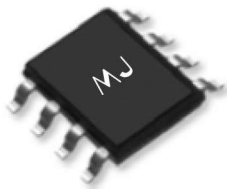
- ◆ Power switching application
- ◆ Load switch



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ5015S	MJ5015S	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (Tc=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	50	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	15	A
Drain Current-Continuous($T_c = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	10.6	A
Pulsed Drain Current	I_{DM}	30	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	42	℃/W
---	-----------------	----	-----

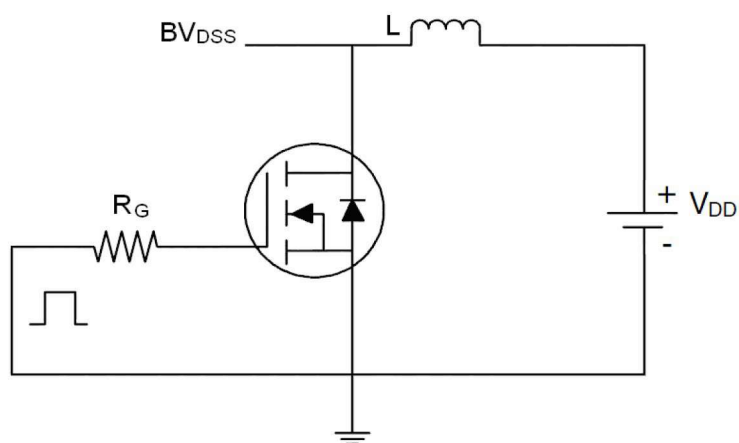
Electrical Characteristics (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V,I _b =250μA	50	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =50V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _b =250μA	0.9	1.2	1.8	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _b =12A	-	5.7	7.6	mΩ
		V _{GS} =4.5V, I _b =6A	-	6.3	8.0	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _b =12A	40	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V F=1.0MHz	-	4100	-	PF
Output Capacitance	C _{oss}		-	298	-	PF
Reverse Transfer Capacitance	C _{rss}		-	229	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V,R _L =1Ω V _{GS} =10V,R _{GEN} =3Ω	-	8.5	-	nS
Turn-on Rise Time	t _r		-	7	-	nS
Turn-Off Delay Time	t _{d(off)}		-	40	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _b =12A V _{GS} =10V	-	93	-	nC
Gate-Source Charge	Q _{gs}		-	9.7	-	nC
Gate-Drain Charge	Q _{gd}		-	20	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _s =15A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _s		-	-	15	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =15A di/dt= 100A/μs ^(Note 3)	-	32	-	nS
Reverse Recovery Charge	Q _{rr}		-	45	-	nC

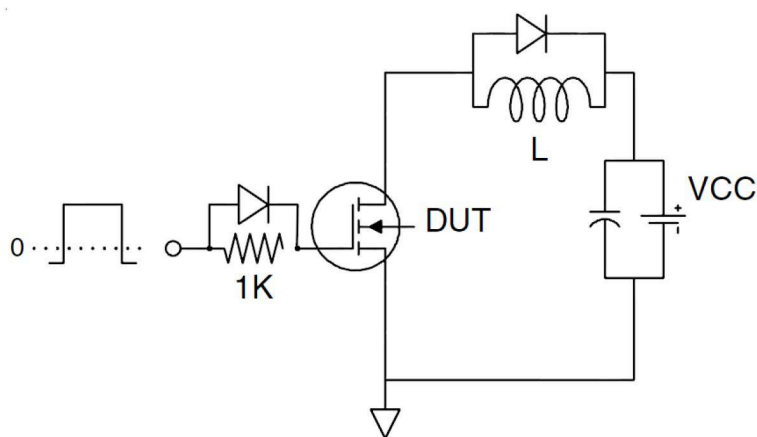
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production

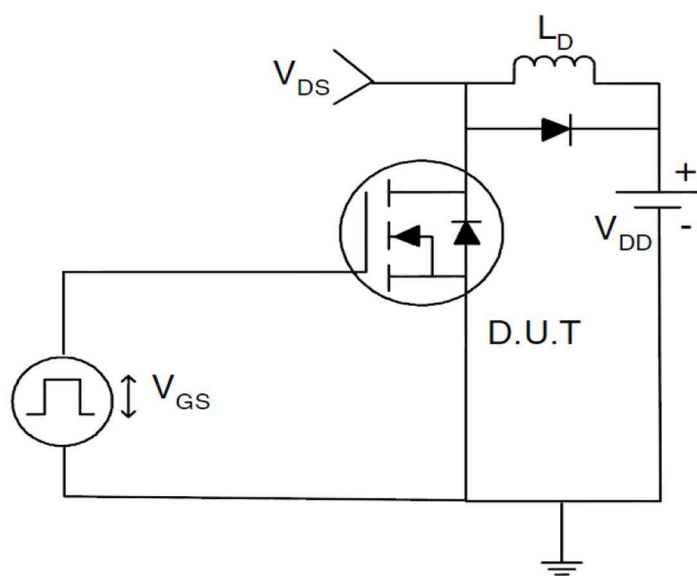
Test circuit



EAS test Circuit

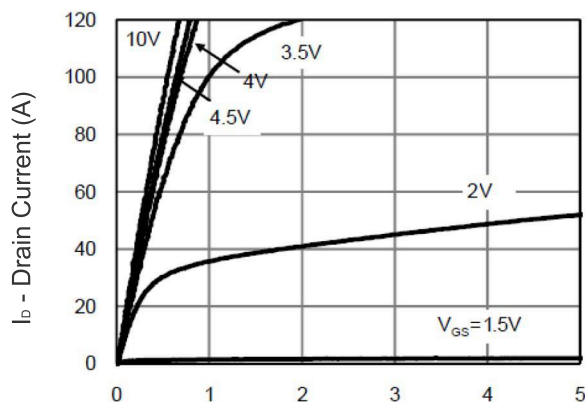


Gate charge test Circuit

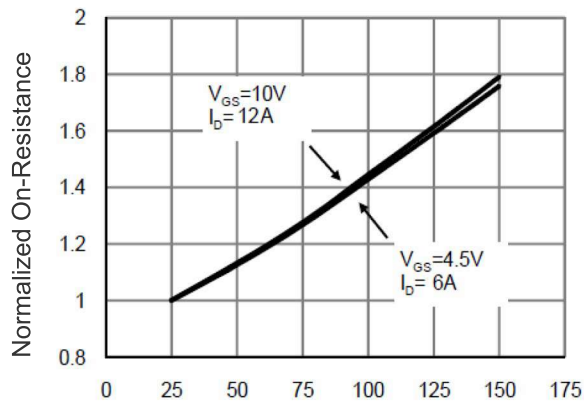


Switch Time Test Circuit

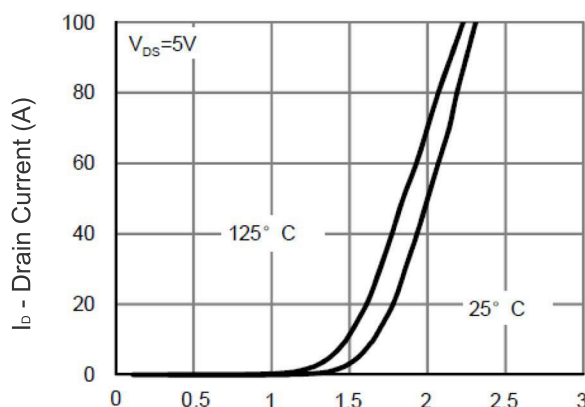
Typical Electrical and Thermal Characteristics (Curves)



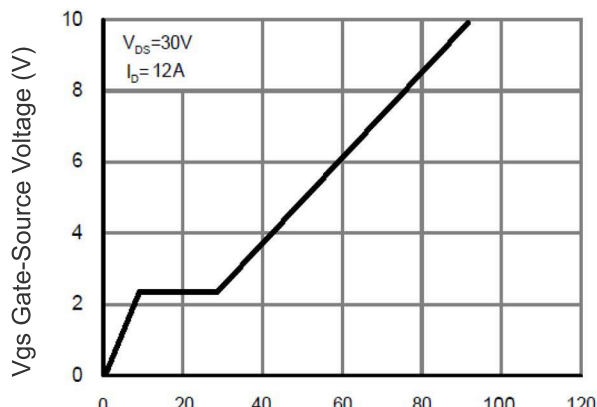
V_{DS} Drain-Source Voltage (V)
Figure 1 Output Characteristics



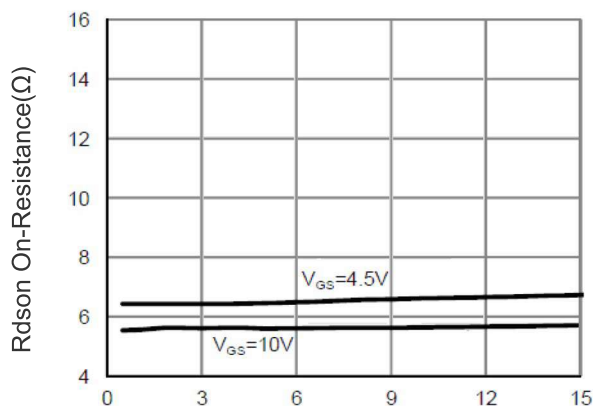
T_J -Junction Temperature(°C)
Figure 4 $R_{DS(on)}$ -Junction Temperature



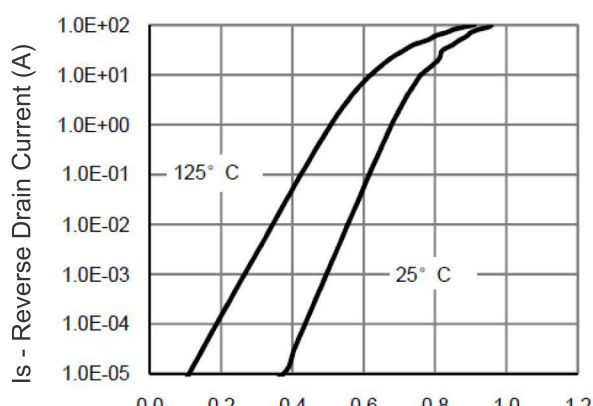
V_{GS} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



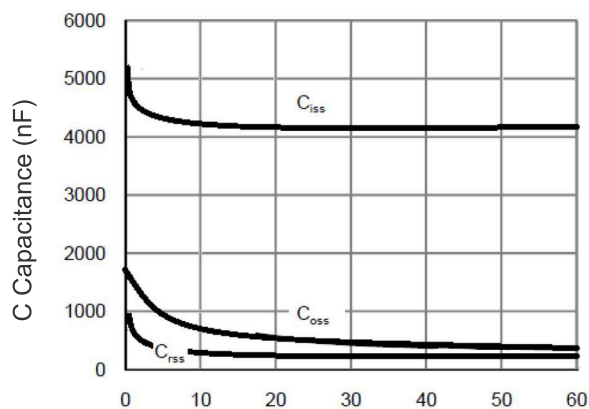
Q_g Gate Charge (nC)
Figure 5 Gate Charge



I_D - Drain Current (A)
Figure 3 $R_{DS(on)}$ - Drain Current

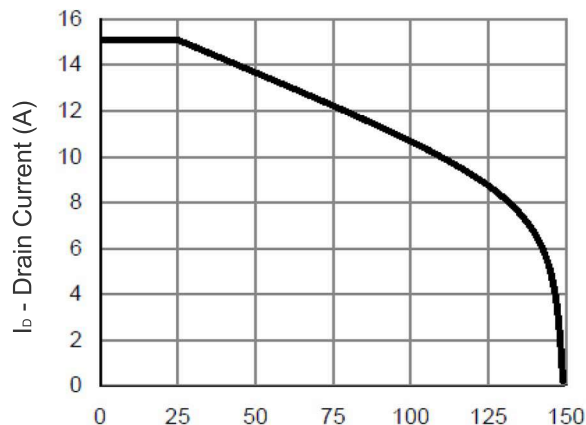


V_{SD} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



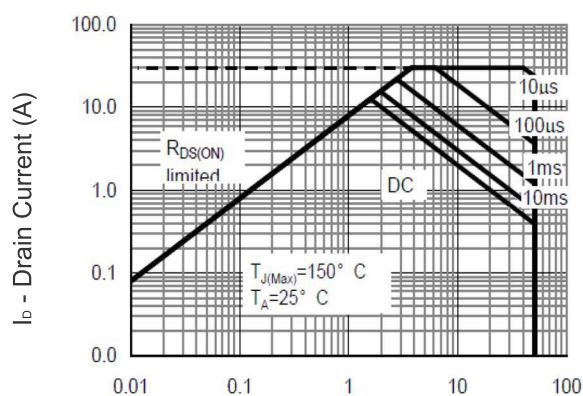
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



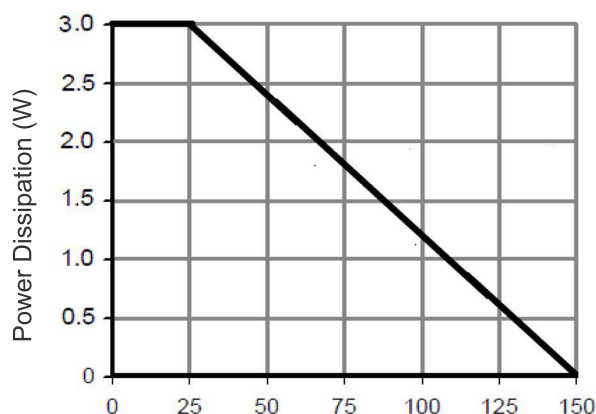
Tj - Junction Temperature(°C)

Figure 9 Current De-rating



Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tj - Junction Temperature(°C)

Figure 10 Power De-rating

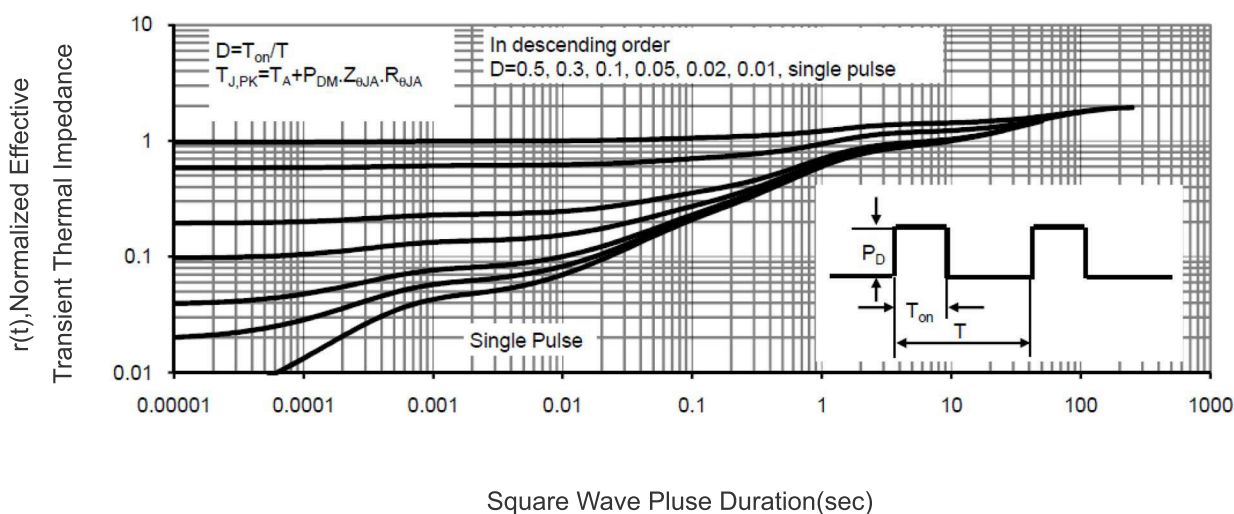
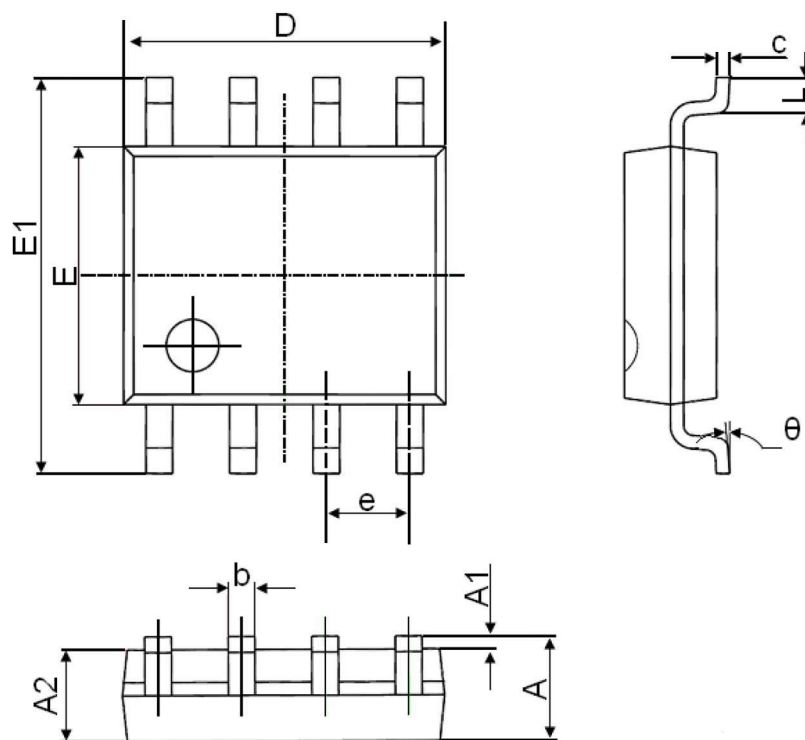


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Attention:

Any and all MJ power products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MJ power representative nearest you before using any MJ power products described or contained herein in such applications.

MJ power assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all MJ power products described or contained herein.

Specifications of any and all MJ power products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

MJ power Semiconductor CO.,LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

In the event that any or all MJ power products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MJ power Semiconductor CO.,LTD.

Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MJ power believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the MJ power product that you intend to use.

This catalog provides information as of Sep.2010. Specifications and information herein are subject to change without notice.