

# MJ P-Channel Enhancement Mode Power MOSFET

## Description

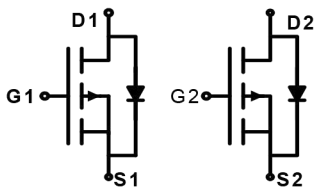
The MJ4953 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.

## General Features

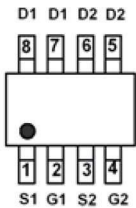
- ◆  $V_{DS} = -30V, I_D = -5.1A$   
 $R_{DS(ON)} < 90m\Omega @ V_{GS} = -4.5V$   
 $R_{DS(ON)} < 55m\Omega @ V_{GS} = -10V$
- ◆ High power and current handing capability
- ◆ Lead free product is acquired
- ◆ Surface Mount Package

## Application

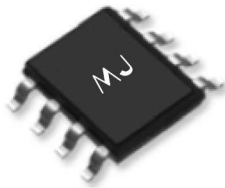
- ◆ PWM applications
- ◆ Load switch
- ◆ Power management



Schematic diagram



Marking and pin assignment



SOP-8 top view

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
4953	MJ4953	SOP-8	Ø330mm	12mm	2500 units

## Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous	$I_D$	-5.1	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	-20	A
Maximum Power Dissipation	$P_D$	2.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	℃

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	50	℃/W
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Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.1	-1.6	-2.1	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5.1A	-	43	55	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.2A	-	62	90	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-4.5A	4	7	-	S
Dynamic Characteristics <sup>(Note 4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V F=1.0MHz	-	520	-	PF
Output Capacitance	C <sub>oss</sub>		-	130	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	70	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-15V, I <sub>D</sub> =-1A V <sub>GS</sub> =-10V, R <sub>GEN</sub> =6Ω	-	7	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	13	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	14	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	9	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-5.1A V <sub>GS</sub> =-10V	-	11	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.2	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-5.1A	-	-	-1.2	V

Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production

## Typical Electrical and Thermal Characteristics

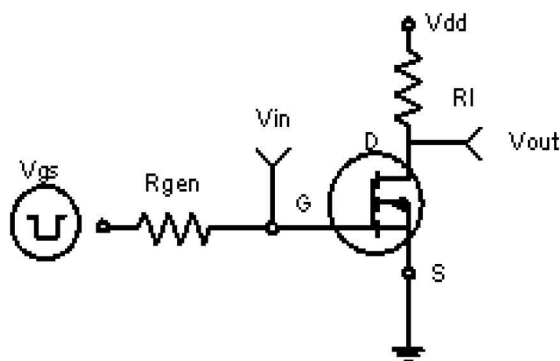


Figure 1 Switching Test Circuit

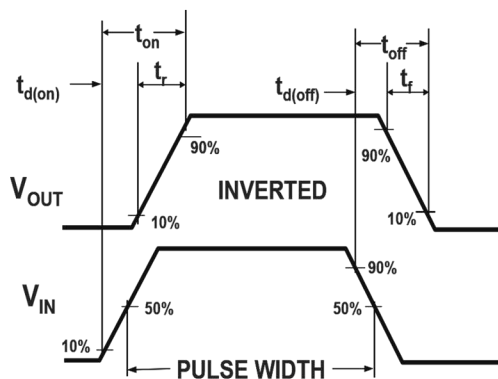
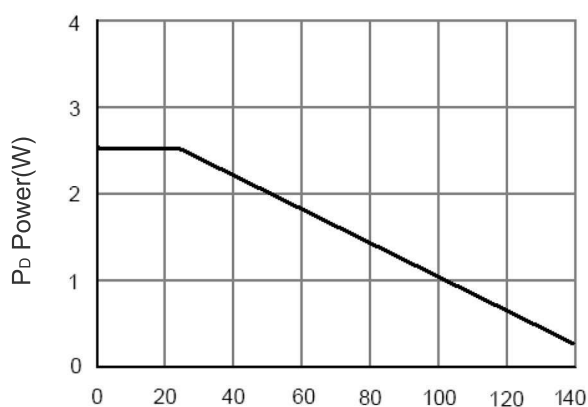
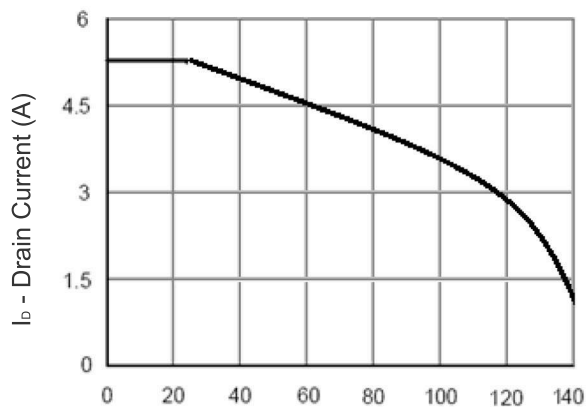


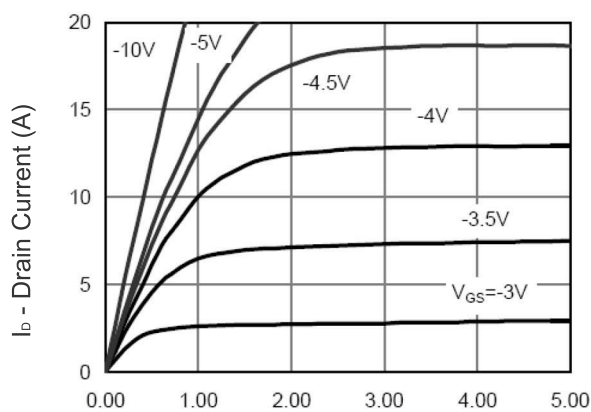
Figure 2 Switching Waveforms



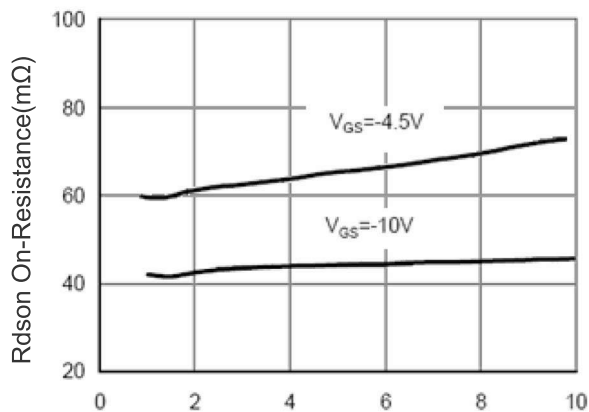
T<sub>J</sub>-Junction Temperature(°C)  
Figure 3 Power Dissipation



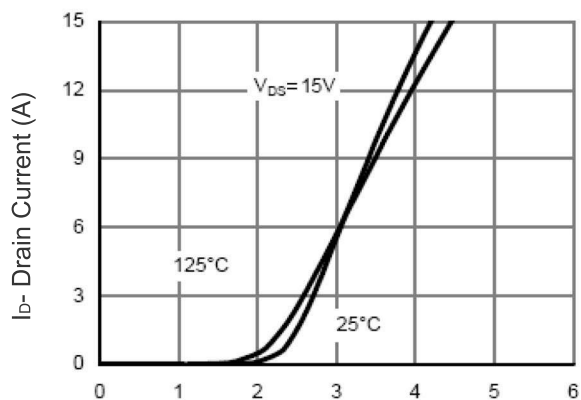
T<sub>J</sub>-Junction Temperature(°C)  
Figure 4 Drain Current



V<sub>DS</sub> Drain-Source Voltage (V)  
Figure 5 Output Characteristics

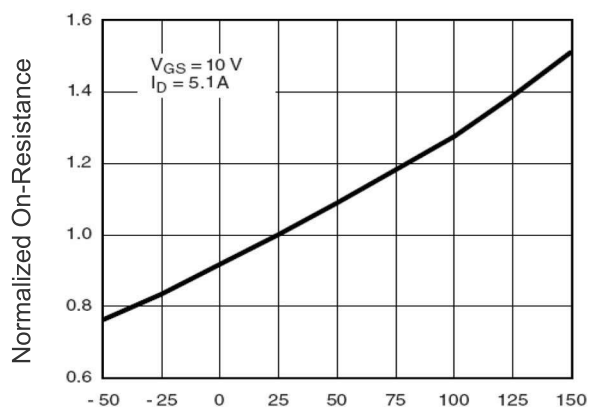


I<sub>D</sub>- Drain Current (A)  
Figure 6 Drain-Source On-Resistance



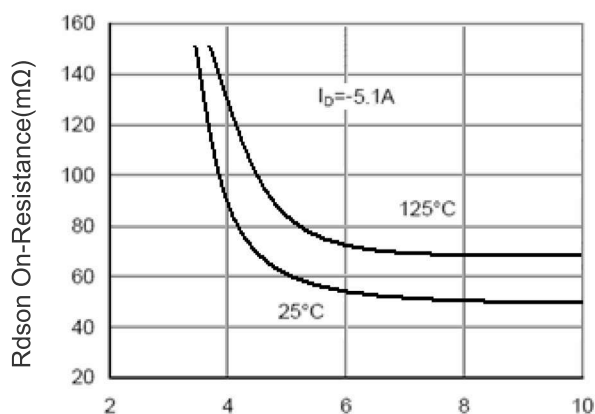
$V_{GS}$  Gate-Source Voltage (V)

Figure 7 Transfer Characteristics



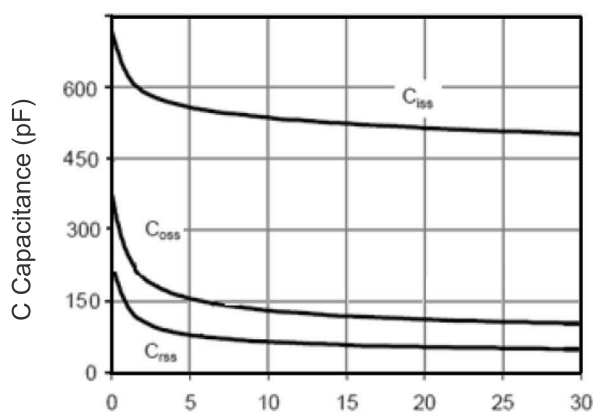
$T_J$ -Junction Temperature(°C)

Figure 8 Drain-Source On-Resistance



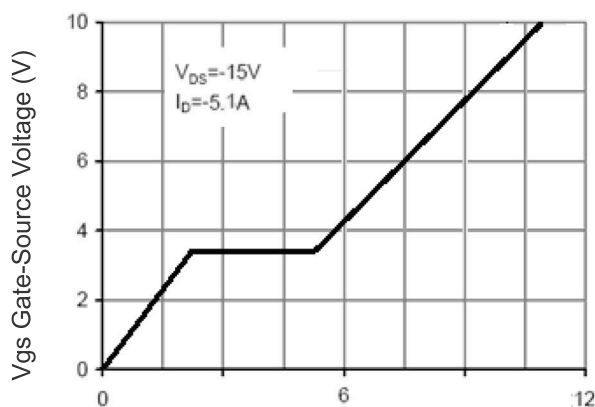
$V_{GS}$  Gate-Source Voltage (V)

Figure 9  $R_{DS(on)}$  vs  $V_{GS}$



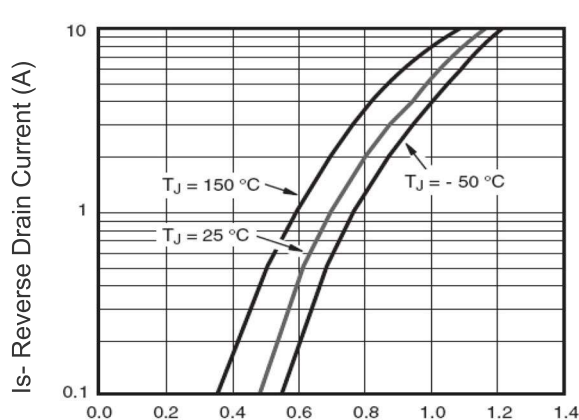
$V_{DS}$  Drain-Source Voltage (V)

Figure10 Capacitance vs  $V_{DS}$



$Q_g$  Gate Charge (nC)

Figure 11 Gate Charge



$V_{SD}$  Source-Drain Voltage (V)

Figure 12 Source- Drain Diode Forward

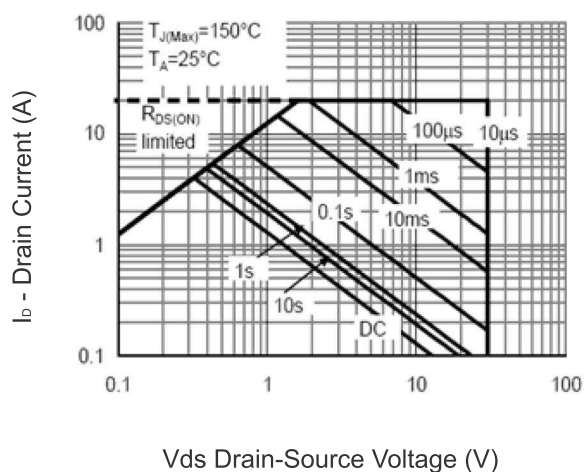


Figure 13 Safe Operation Area

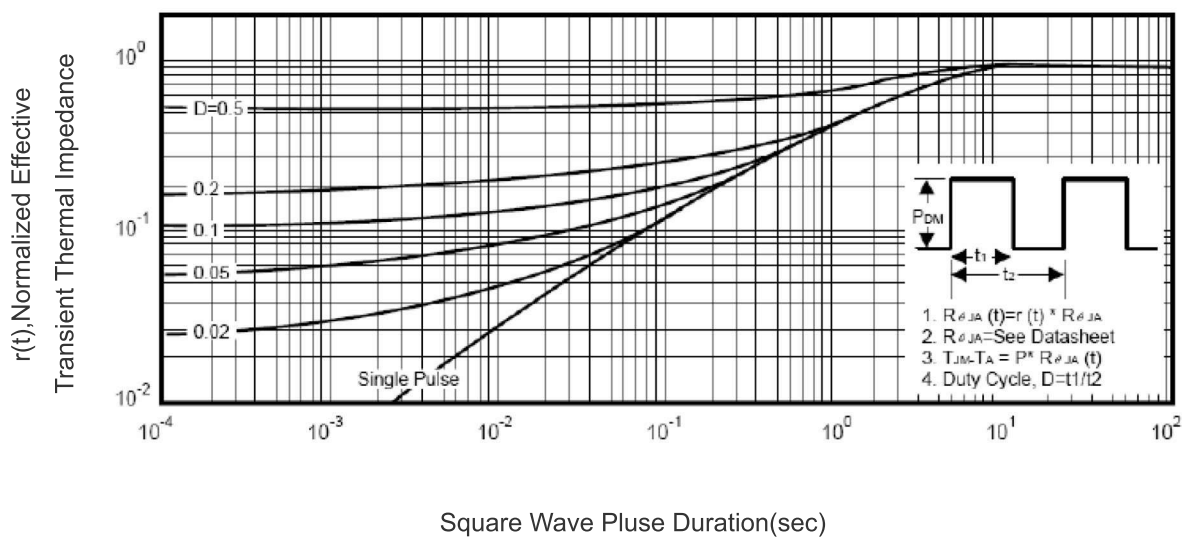
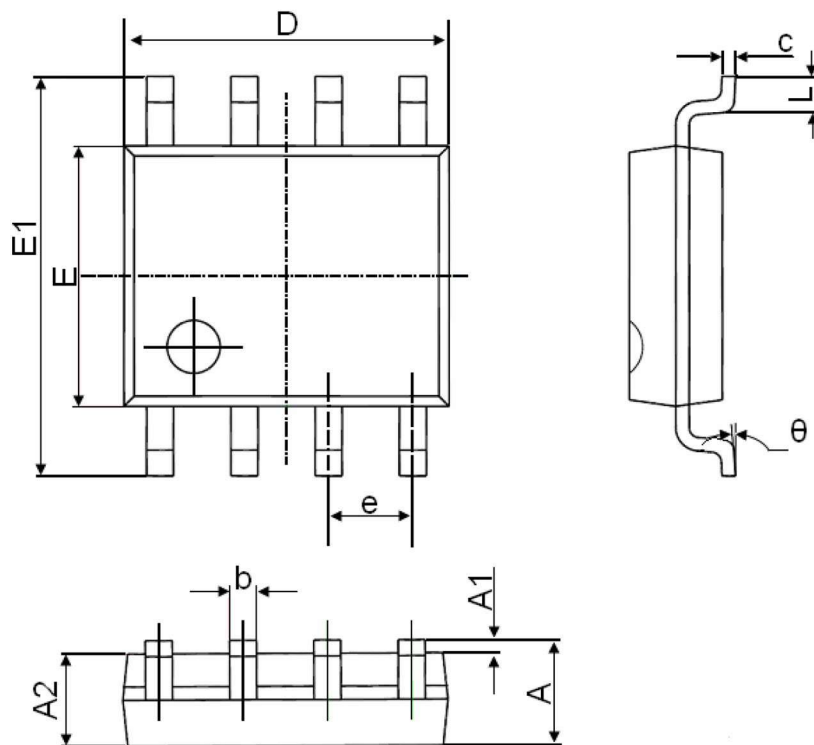


Figure 14 Normalized Maximum Transient Thermal Impedance

# SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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