

MJ P-Channel Enhancement Mode Power MOSFET

Description

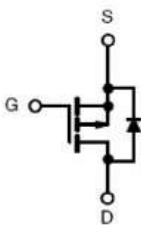
The MJ40P70K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge . This device is well suited for high current load applications.

General Features

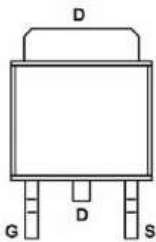
- ◆ $V_{DS} = -40V, I_D = -70A$
 $R_{DS(ON)} < 10m\Omega @ V_{GS} = -10V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high EAS
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

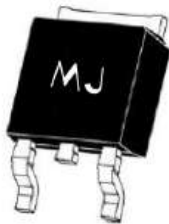
- ◆ Power switch
- ◆ Load switch in high current applications
- ◆ DC/DC converters



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ40P70K	MJ40P70K	TO-252-2L	330mm	-	2500PCS

Absolute Maximum Ratings ($T_c = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-70	A
Drain Current-Continuous($T_c = 100^{\circ}\text{C}$)	$I_{D(100^{\circ}\text{C})}$	-49.5	A
Pulsed Drain Current	I_{DM}	-200	A
Maximum Power Dissipation	P_D	130	W
Derating factor		1.04	W/ $^{\circ}\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1012	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.96	$^{\circ}\text{C/W}$
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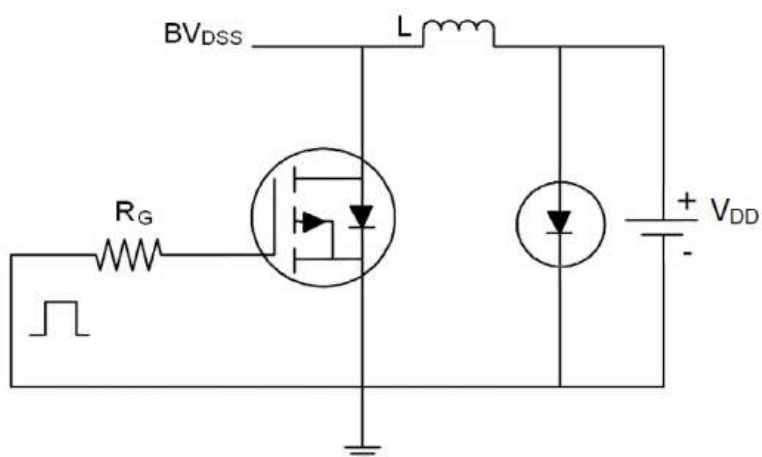
Electrical Characteristics (T_c =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A	-	7.5	10	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-10V,I _D =-20A	-	50	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =-20V,V _{GS} =0V F=1.0MHz	-	5380	-	PF
Output Capacitance	C _{oss}		-	570	-	PF
Reverse Transfer Capacitance	C _{rss}		-	500	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V, R _L =2Ω V _{GS} =-10V,R _G =1Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	18	-	nS
Total Gate Charge	Q _g	V _{DS} =-20V,I _D =-20A V _{GS} =-10V	-	106	-	nC
Gate-Source Charge	Q _{gs}		-	22	-	nC
Gate-Drain Charge	Q _{gd}		-	27	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =-70A	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	-70	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =-70A di/dt=-100A/μs <small>(Note 3)</small>	-	53	-	nS
Reverse Recovery Charge	Q _{rr}		-	50	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

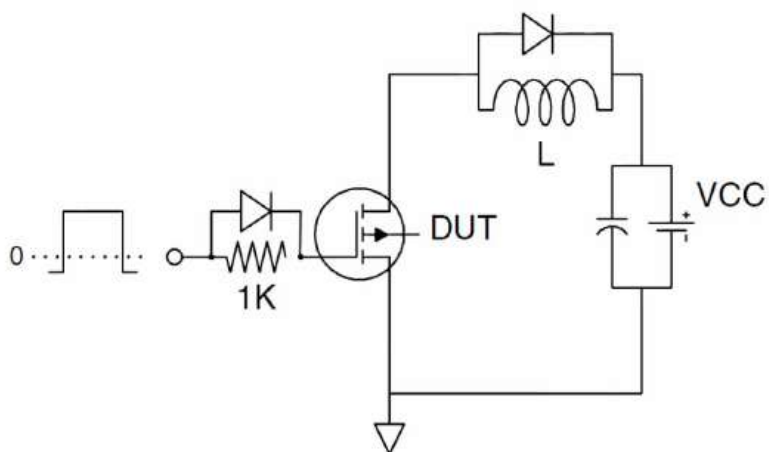
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition: T_J=25℃,V_{DD}=-20V,V_G=-10V,L=1mH,R_G=25Ω,I_{AS}=45A

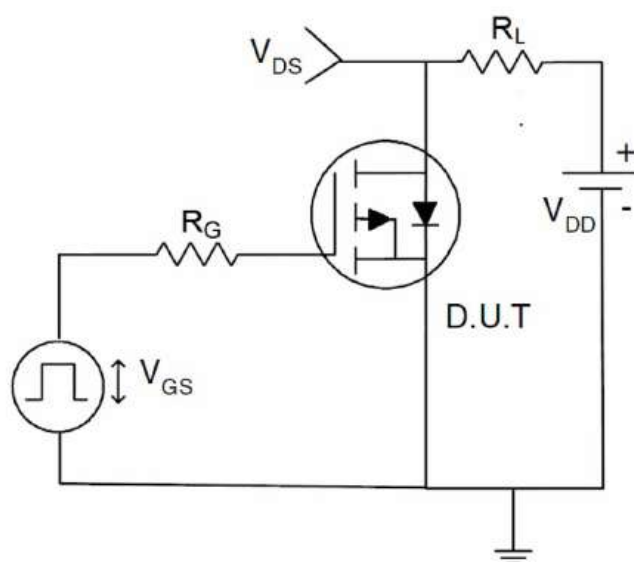
Test circuit



EAS test Circuit

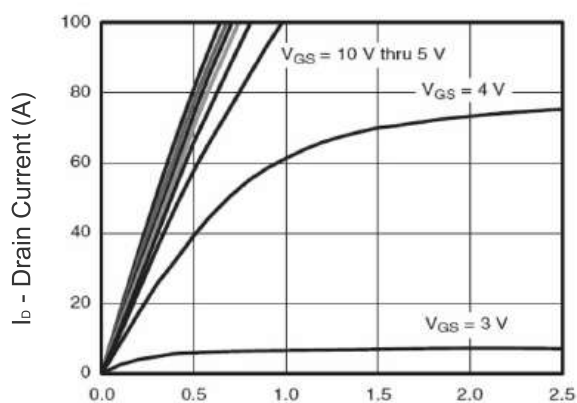


Gate charge test Circuit



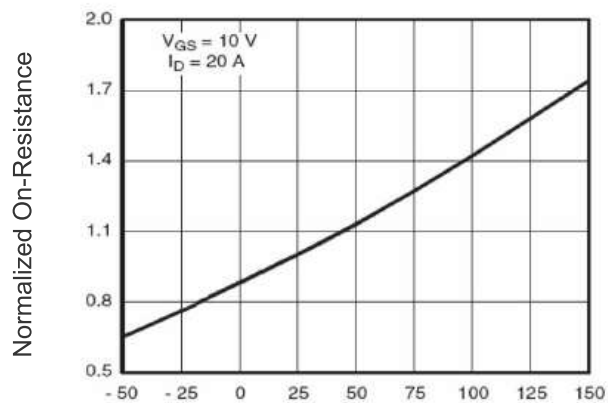
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



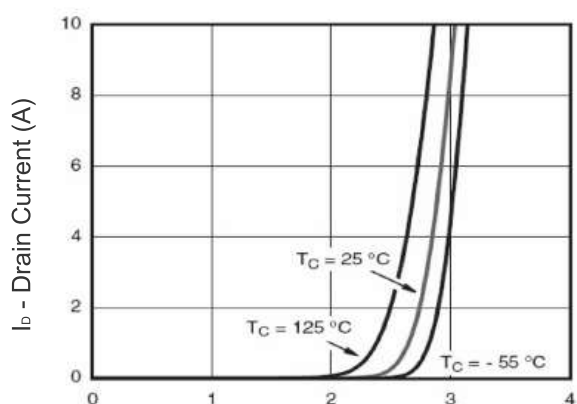
V_{DS} Drain-Source Voltage (V)

Figure 1 Output Characteristics



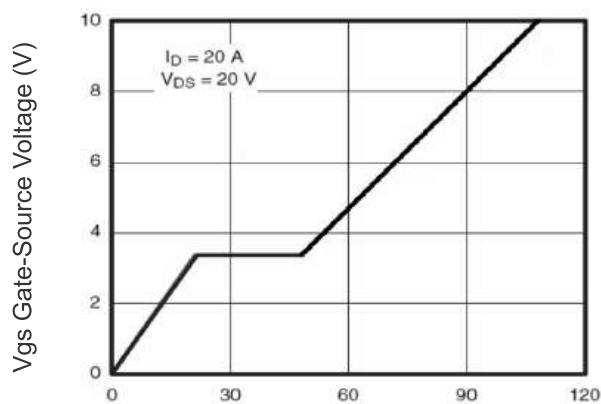
T_J -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



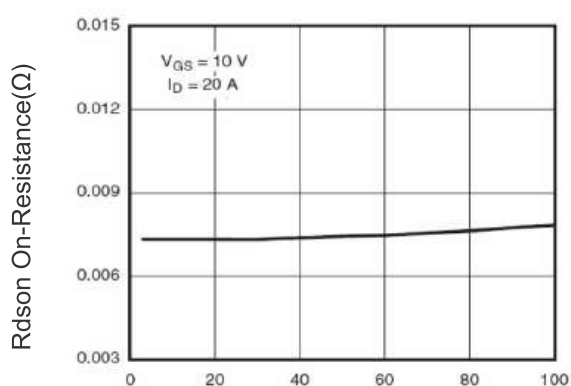
V_{GS} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



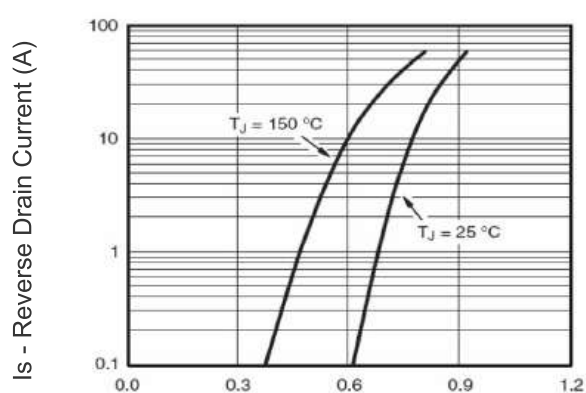
Q_g Gate Charge (nC)

Figure 5 Gate Charge



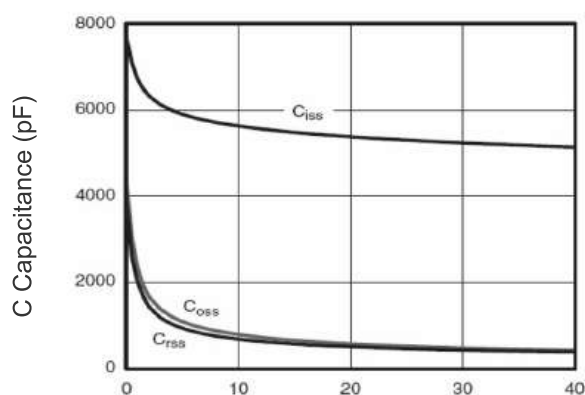
I_D - Drain Current (A)

Figure 3 Rdson- Drain Current

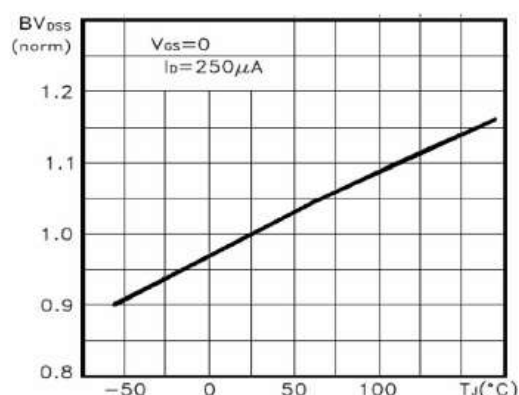


V_{SD} Source-Drain Voltage (V)

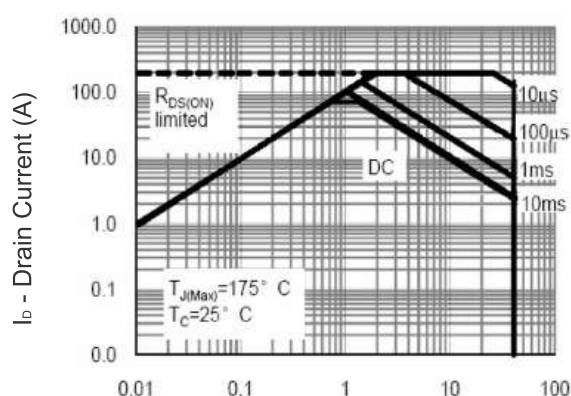
Figure 6 Source- Drain Diode Forward



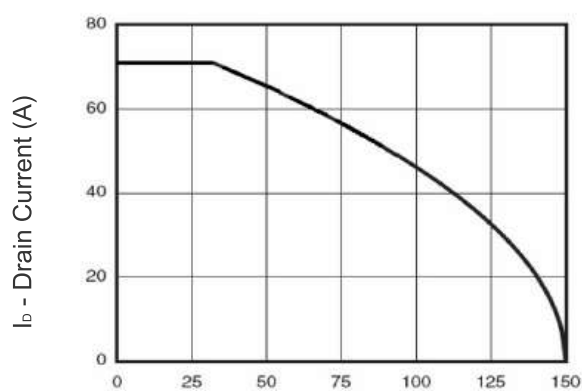
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



Tj -Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)
Figure 10 Id Current Derating vs Junction Temperature

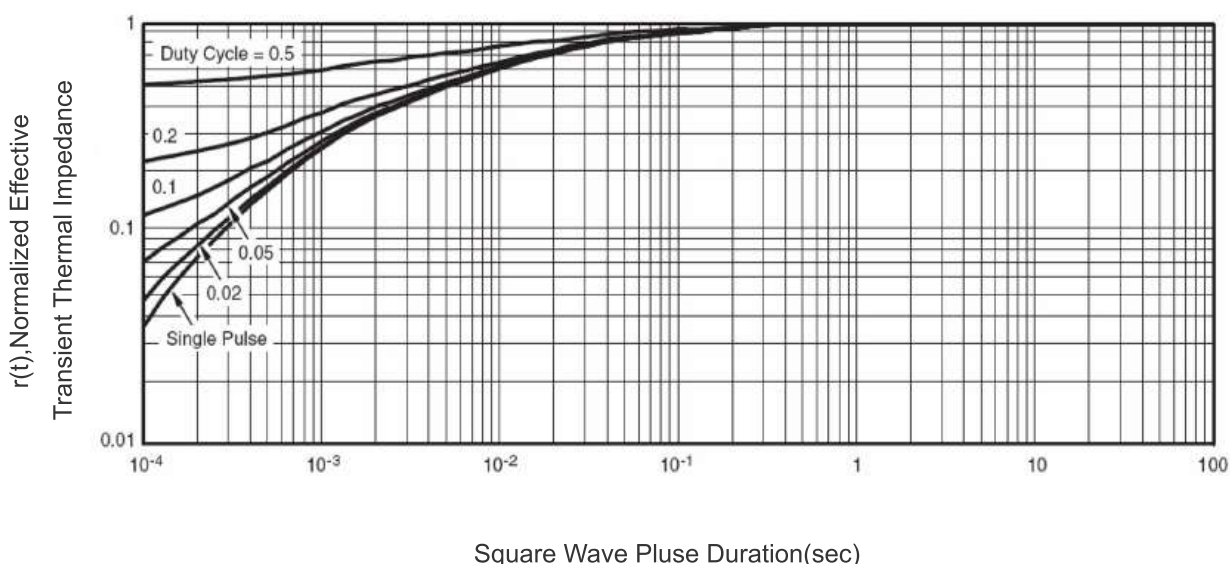
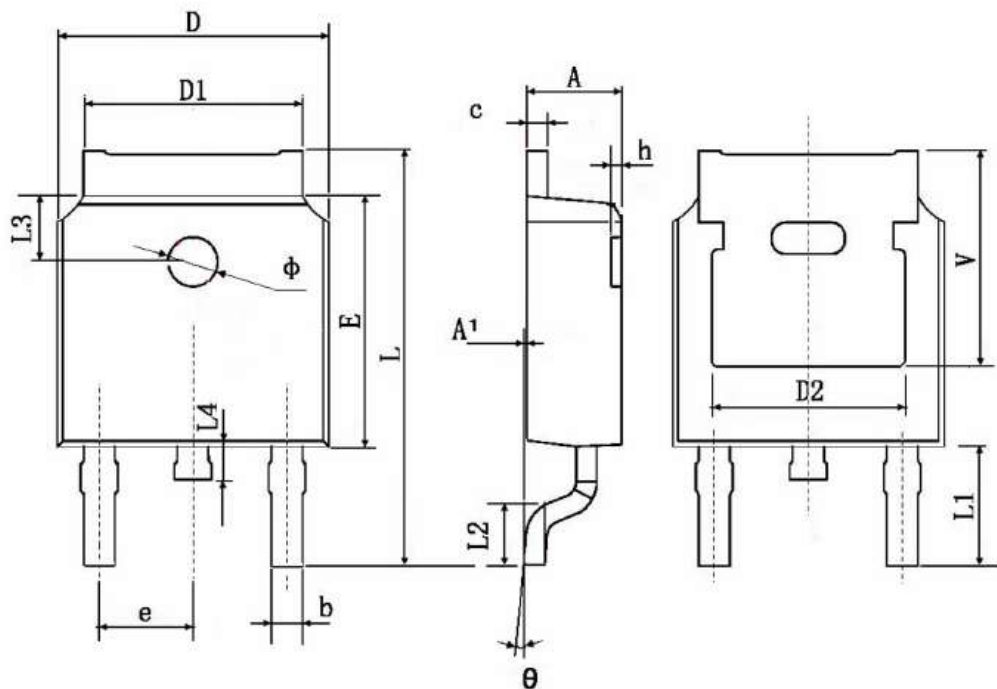


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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