

MJ P-Channel Enhancement Mode Power MOSFET

Description

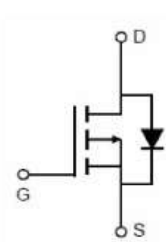
The MJ40P40K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge . This device is well suited for high current load applications.

General Features

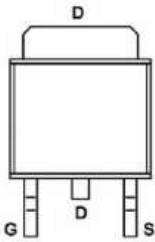
- ◆ $V_{DS} = -40V, I_D = -40A$
 $R_{DS(ON)} < 14m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 24m\Omega @ V_{GS} = -4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation

Application

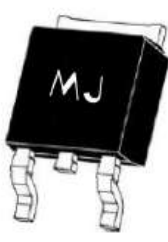
- ◆ Power switching application
- ◆ Hard switched and high frequency circuits
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ40P40K	MJ40P40K	TO-252-2L	-	-	-

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-40	A
Drain Current-Continuous($T_C = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	-28	A
Pulsed Drain Current	I_{DM}	-160	A
Maximum Power Dissipation $T_C = 25^{\circ}C$	P_D	80	W
Derating factor		0.53	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	544	mJ
Drain Source voltage slope, $V_{DS} \leq -32 V$	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq -32 V, I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.88	°C/W
Thermal Resistance,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	°C/W

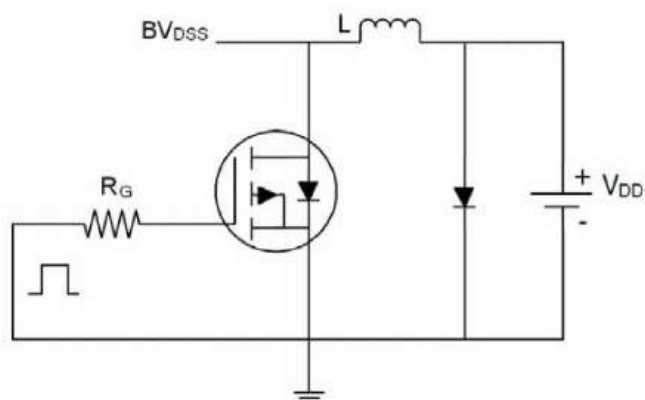
Electrical Characteristics (T_c =25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1.5	-1.9	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-12A	-	12	14	mΩ
		V _{GS} =-4.5V, I _D =-12A	-	18.5	24	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V,I _D =-12A	-	34	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =-20V,V _{GS} =0V F=1.0MHz	-	2960	-	PF
Output Capacitance	C _{oss}		-	370	-	PF
Reverse Transfer Capacitance	C _{rss}		-	310	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V,I _D =-12A V _{GS} =-10V,R _G =3Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	18	-	nS
Turn-Off Delay Time	t _{d(off)}		-	38	-	nS
Turn-Off Fall Time	t _f		-	24	-	nS
Total Gate Charge	Q _g	V _{DS} =-20V,I _D =-12A V _{GS} =-10V	-	42.2	72	nC
Gate-Source Charge	Q _{gs}		-	6.9	-	nC
Gate-Drain Charge	Q _{gd}		-	9.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =-12A	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	-40	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =-12A di/dt=-100A/μs <small>(Note 3)</small>	-	40	-	nS
Reverse Recovery Charge	Q _{rr}		-	42	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

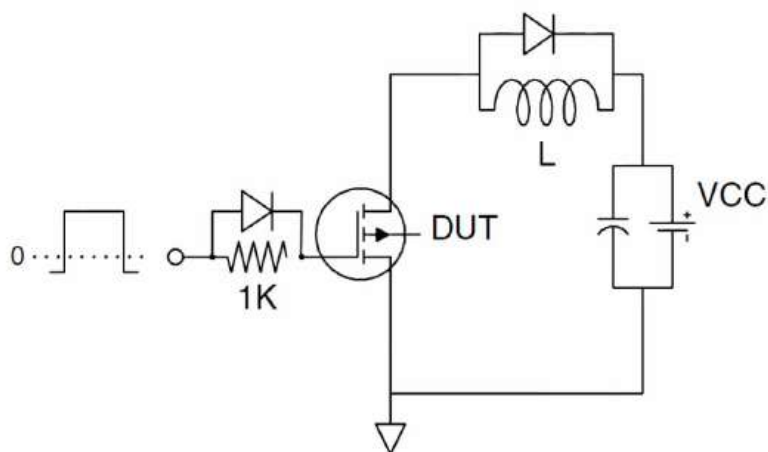
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C, V_{DD}=-20V,V_G=-10V,L=1mH,R_G=25Ω

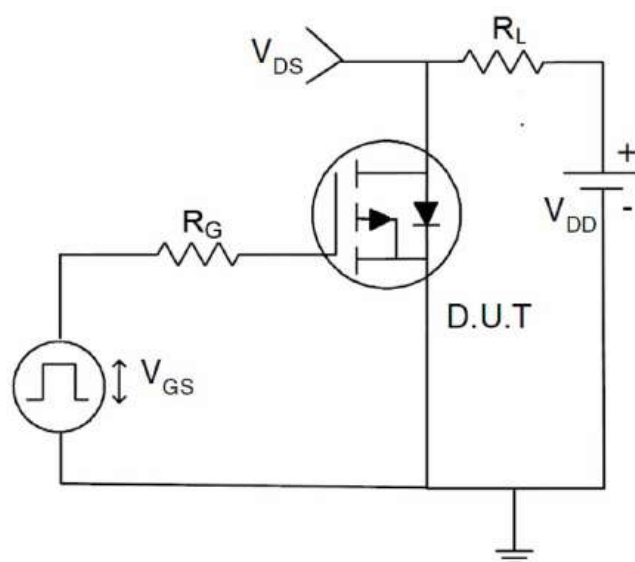
Test circuit



EAS test Circuit

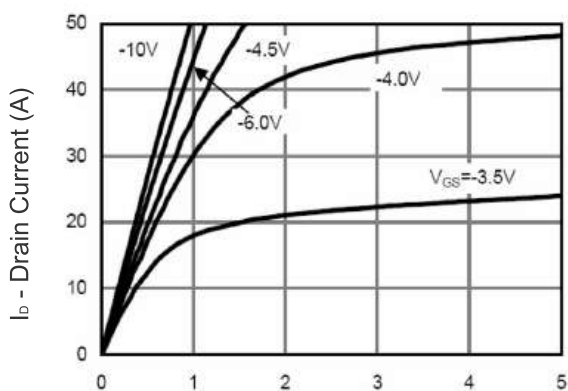


Gate charge test Circuit



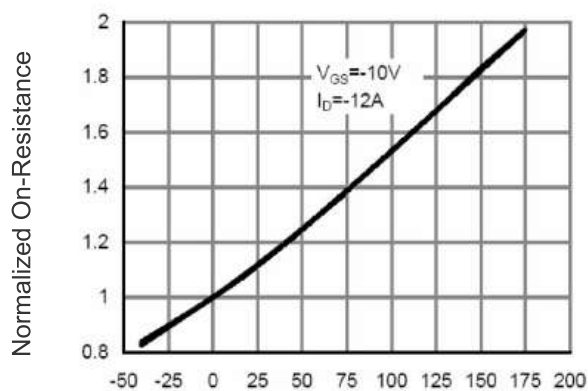
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



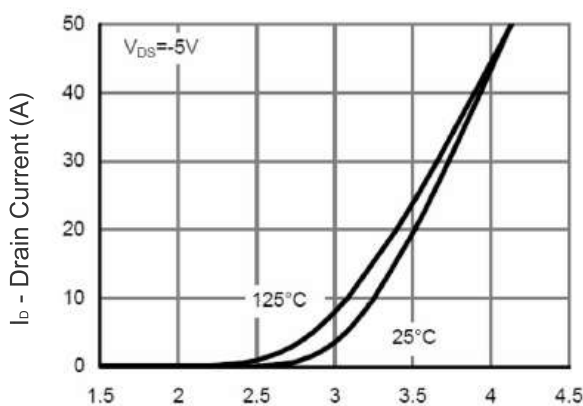
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



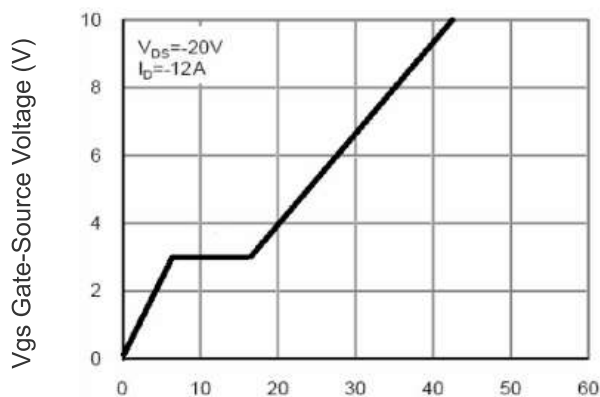
Tj -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



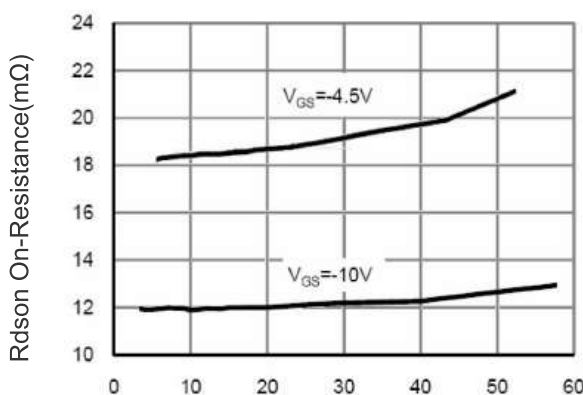
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



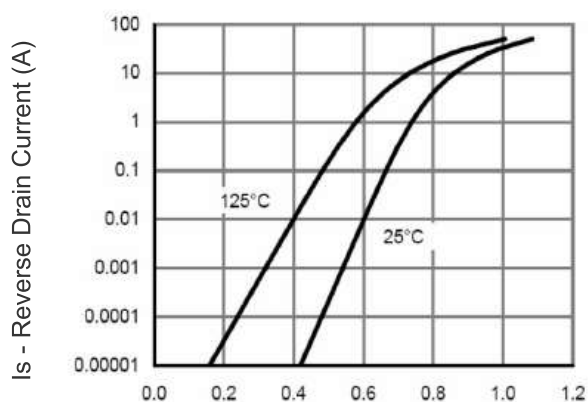
Qg Gate Charge (nC)

Figure 5 Gate Charge



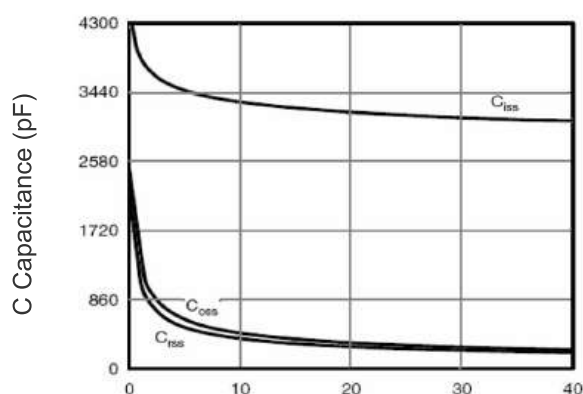
Id - Drain Current (A)

Figure 3 Rdson- Drain Current



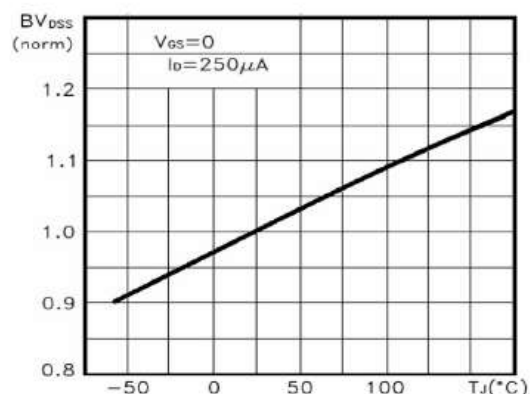
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



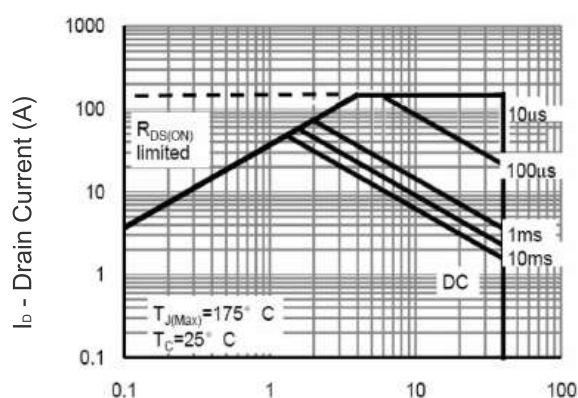
-Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



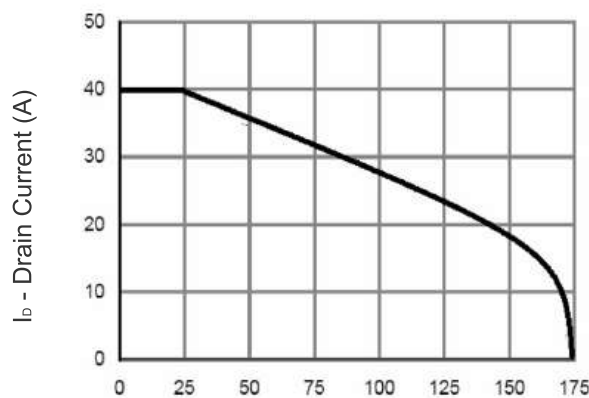
Tj -Junction Temperature(°C)

Figure 9 BVdss vs Junction Temperature



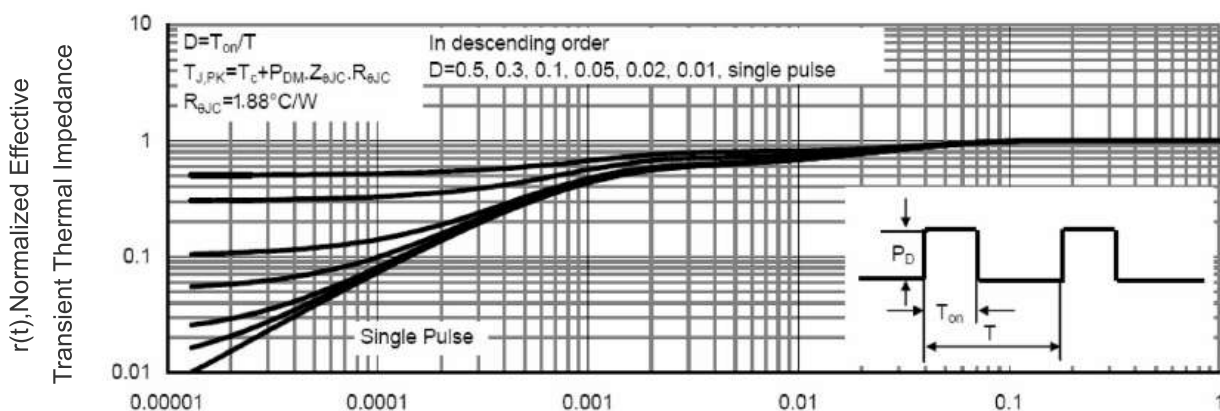
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)

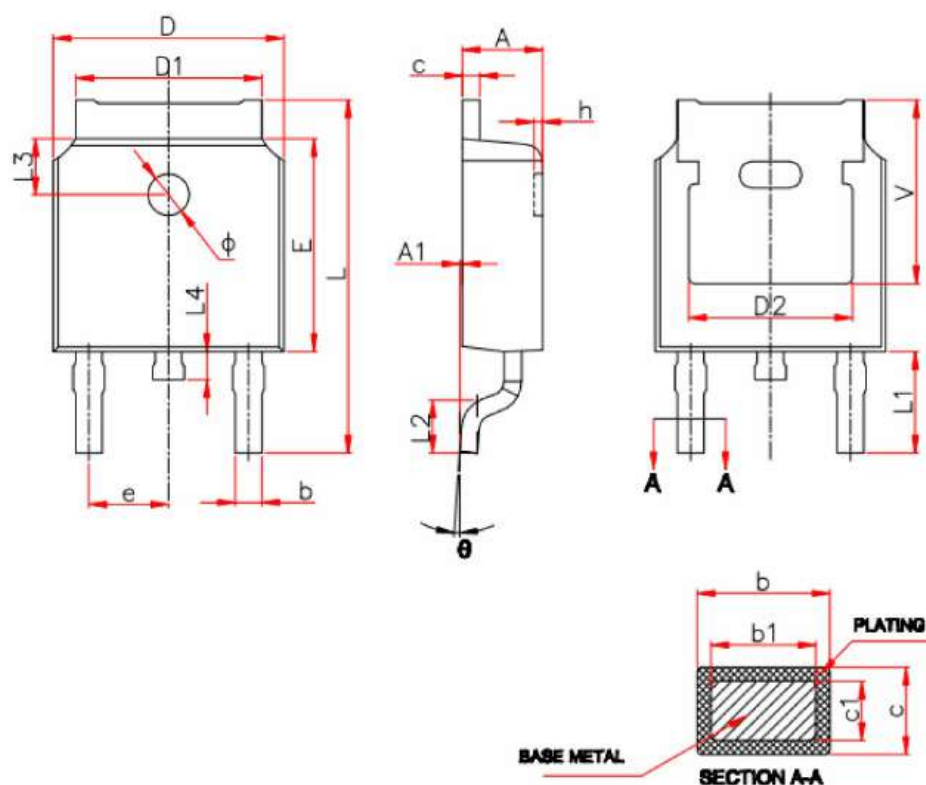
Figure 10 Id Current Derating vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
ϕ	1.10	1.30
θ	0°	8°

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