

# MJ P-Channel Enhancement Mode Power MOSFET

## Description

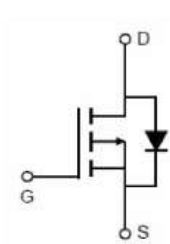
The MJ40P15K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge . This device is well suited for use as a load switch or in PWM applications.

## General Features

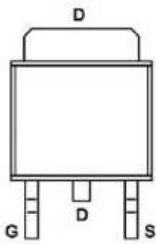
- ◆  $V_{DS} = -40V, I_D = -15A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = -4.5V$
- ◆ High density cell design for ultra low  $R_{dson}$
- ◆ Fully characterized avalanche voltage and current
- ◆ Excellent package for good heat dissipation

## Application

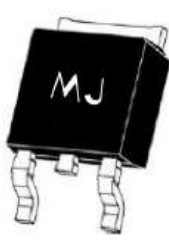
- ◆ Load switch
- ◆ PWM application



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100%  $\Delta V_{ds}$  TESTED!

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ40P15K	MJ40P15K	TO-252-2L	-	-	-

## Absolute Maximum Ratings (Tc =25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-15	A
Pulsed Drain Current	$I_{DM}$	-60	A
Maximum Power Dissipation	$P_D$	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	°C

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3.0	°C/W
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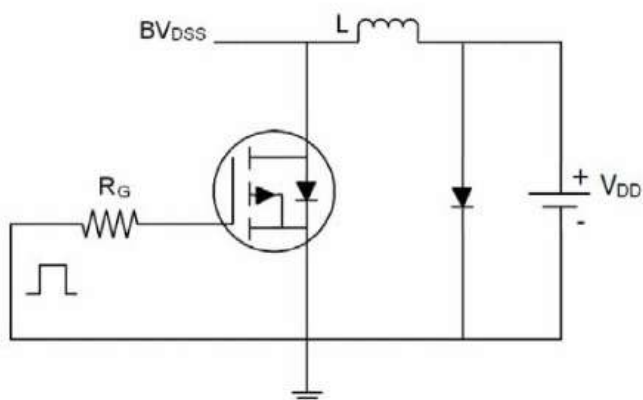
Electrical Characteristics (T<sub>c</sub> =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-40V,V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =±20V,V <sub>GS</sub> =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =-250μA	-1.0	-1.5	-2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A	-	29	35	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-10A	-	34	45	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V,I <sub>D</sub> =-15A	-	10	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-20V,V <sub>GS</sub> =0V F=1.0MHz	-	930	-	PF
Output Capacitance	C <sub>oss</sub>		-	85	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	35	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-20V, R <sub>L</sub> =1Ω V <sub>GS</sub> =-10V,R <sub>G</sub> =3Ω	-	8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	4	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	32	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	7	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-20V,I <sub>D</sub> =-15A V <sub>GS</sub> =-10V	-	25	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =-15A	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	I <sub>S</sub>		-	-	-15	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> =25°C, I <sub>F</sub> =-15A di/dt=-100A/μs <small>(Note 3)</small>	-	25	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	31	-	nC

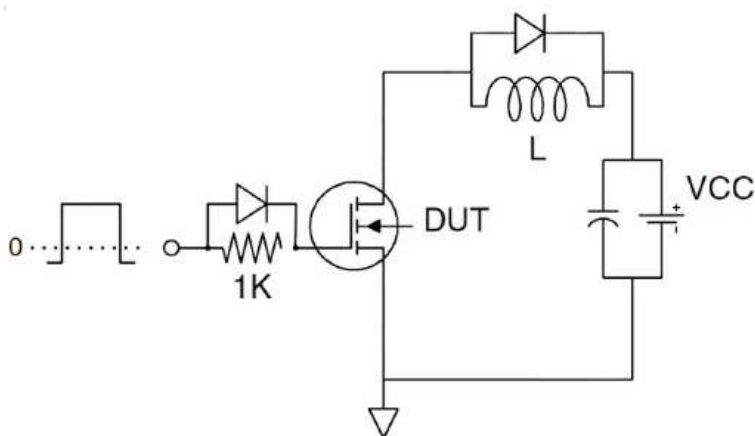
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production

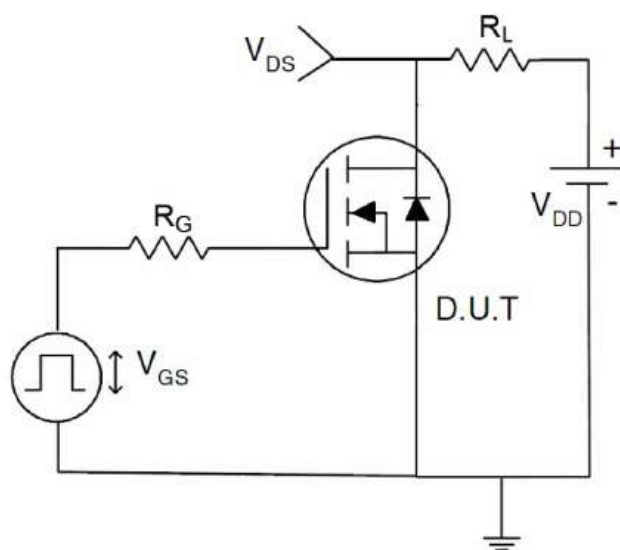
## Test circuit



EAS test Circuit

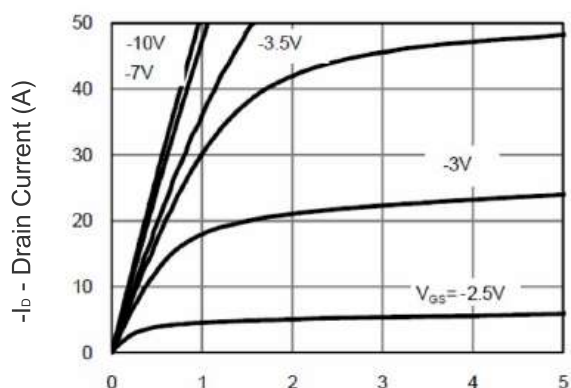


Gate charge test Circuit



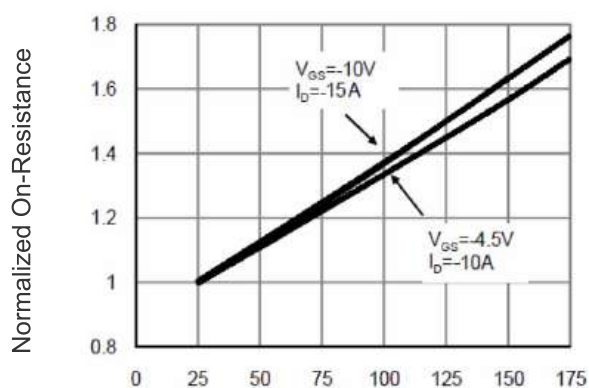
Switch Time Test Circuit

# P- Channel Typical Electrical and Thermal Characteristics (Curves)



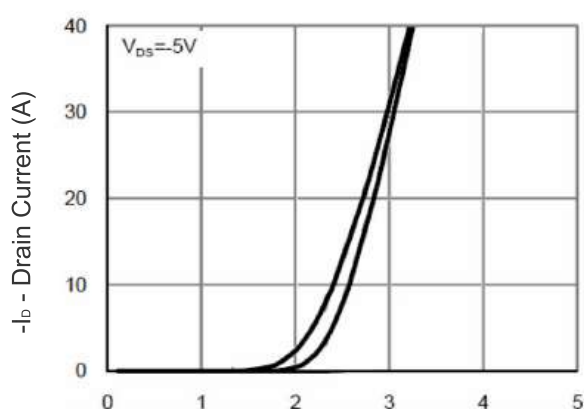
-Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



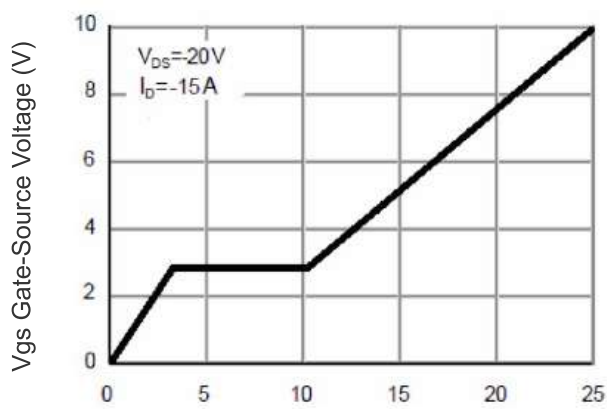
Tj - Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



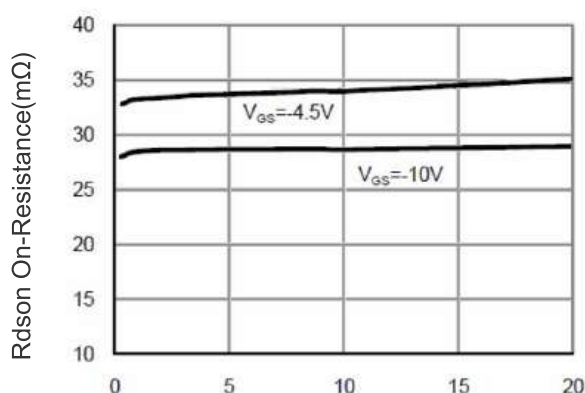
-Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



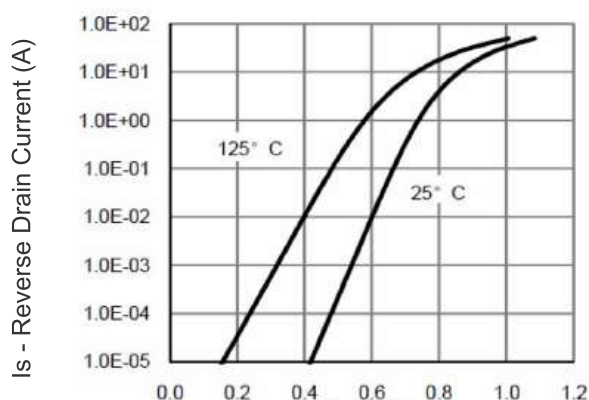
Qg Gate Charge (nC)

Figure 5 Gate Charge



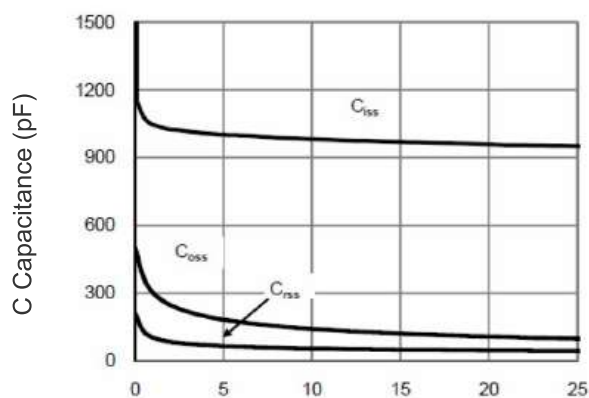
-Ib - Drain Current (A)

Figure 3 Rdson- Drain Current

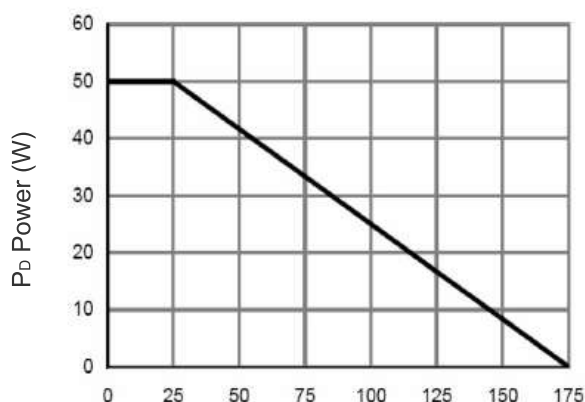


-Vsd Source-Drain Voltage (V)

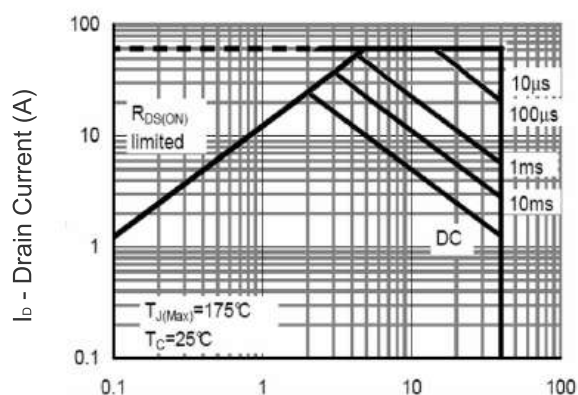
Figure 6 Source- Drain Diode Forward



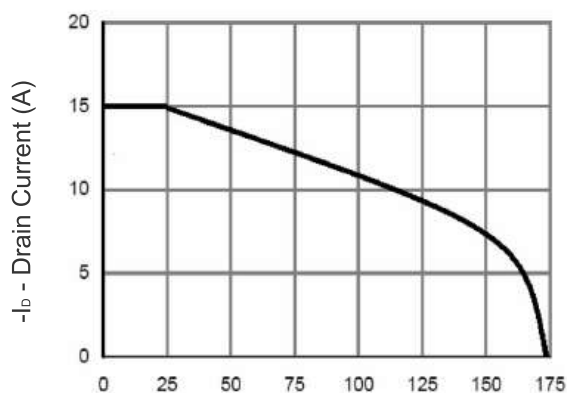
-Vds Drain-Source Voltage (V)  
Figure 7 Capacitance vs Vds



Tj -Junction Temperature(°C)  
Figure 9 Power Dissipation



-Vds Drain-Source Voltage (V)  
Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)  
Figure 10 Id Current De-rating

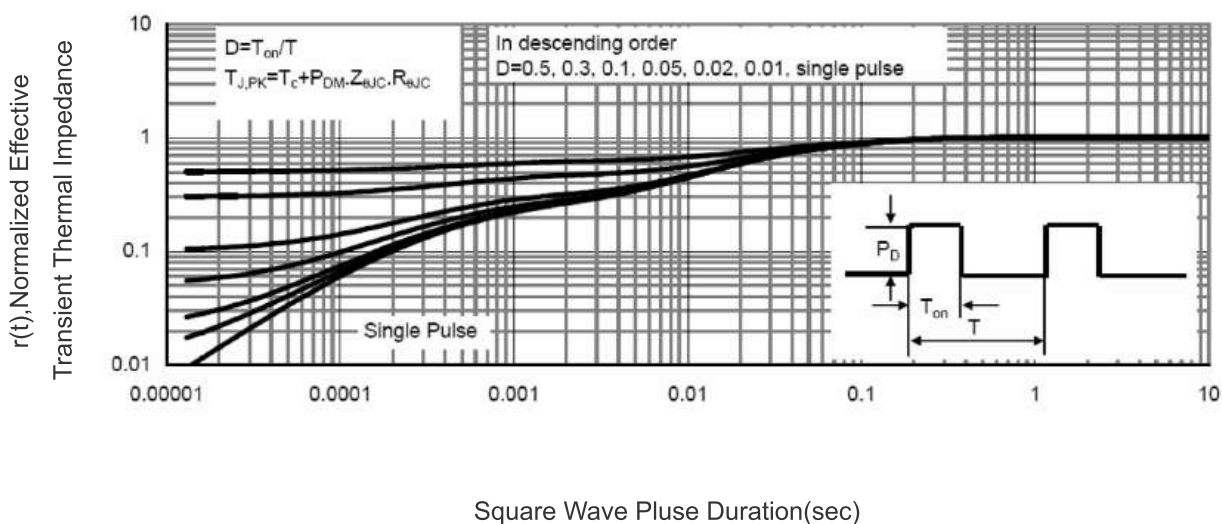
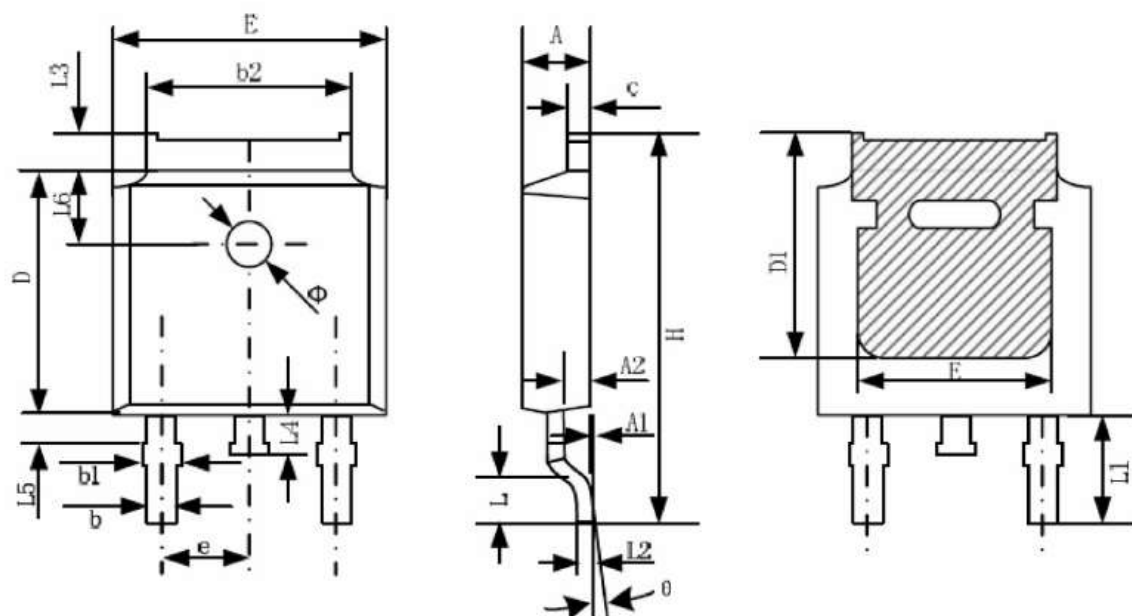


Figure 11 Normalized Maximum Transient Thermal Impedance

## TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
$\Phi$	1.20	1.40	0.047	0.055
$\theta$	0°	8°	0°	8°



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