

MJ N-Channel Enhancement Mode Power MOSFET

Description

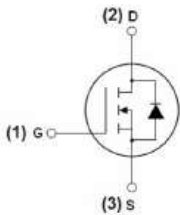
The MJ40H29D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

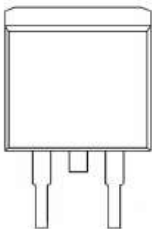
- ◆ $V_{DS}=40V, I_D=290A$
 $R_{DS(ON)} < 2.4m\Omega @ V_{GS}=10V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

- ◆ Power switching application
- ◆ Hard switched and High frequency circuits
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-263-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ40H29D	MJ40H29D	TO-263-2L	-	-	-

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	290	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_{D(100^{\circ}C)}$	205	A
Pulsed Drain Current	I_{DM}	840	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/ $^{\circ}C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	2500	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.48	$^{\circ}C/W$
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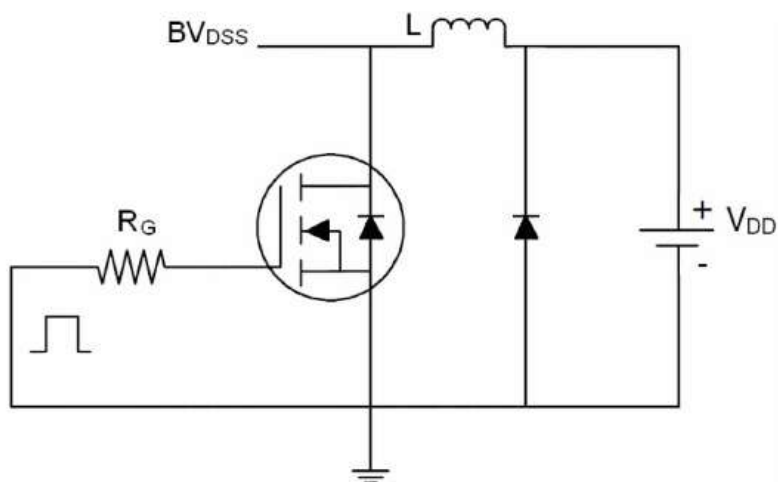
Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V, V _{GS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.3	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	1.9	2.4	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =40A	-	100	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V F=1.0MHz	-	10331	-	PF
Output Capacitance	C _{oss}		-	1160	-	PF
Reverse Transfer Capacitance	C _{rss}		-	1045	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =15Ω R _G =2.5Ω, V _{GS} =10V	-	41	-	nS
Turn-on Rise Time	t _r		-	40	-	nS
Turn-Off Delay Time	t _{d(off)}		-	145	-	nS
Turn-Off Fall Time	t _f		-	65	-	nS
Total Gate Charge	Q _g	I _D =20A, V _{DD} =20V V _{GS} =10V	-	239	-	nC
Gate-Source Charge	Q _{gs}		-	23.5	-	nC
Gate-Drain Charge	Q _{gd}		-	49.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	0.85	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	210	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =20A di/dt=100A/μs ^(Note 3)	-	55	-	nS
Reverse Recovery Charge	Q _{rr}		-	90	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

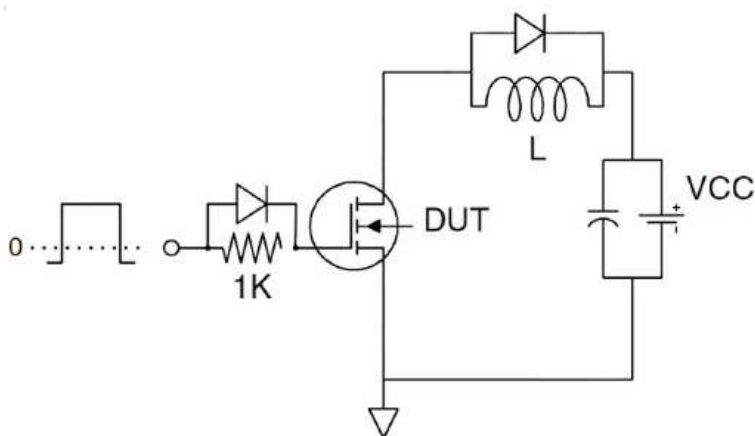
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, $t \leq 10$ sec.
- ③ Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega$

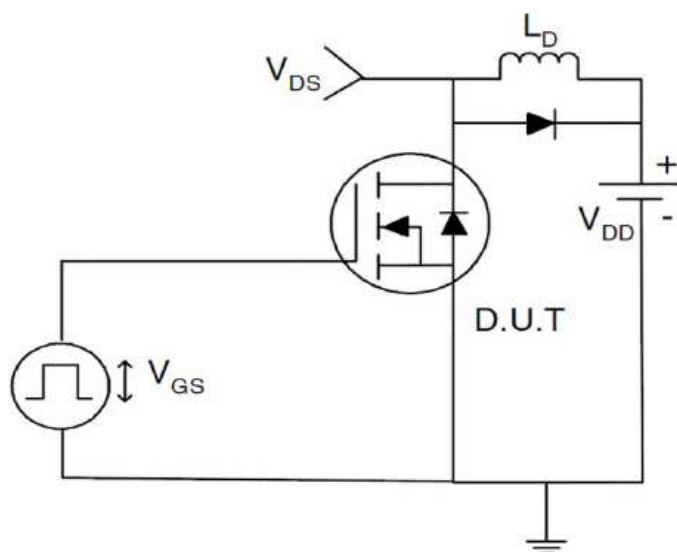
Test circuit



EAS test Circuit

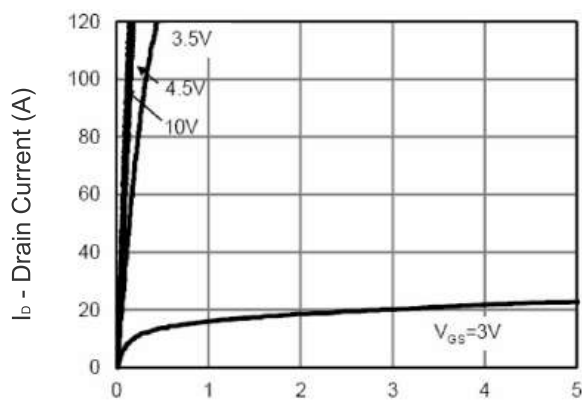


Gate charge test Circuit



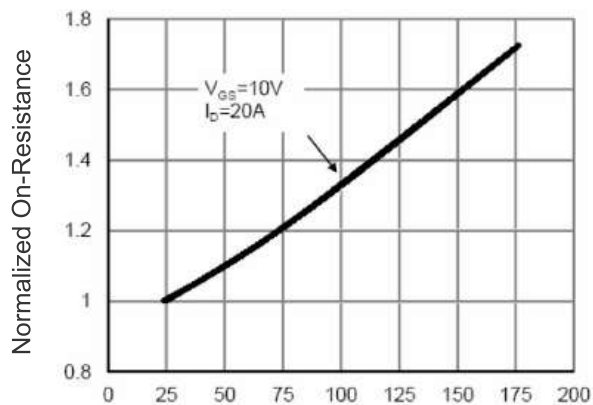
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



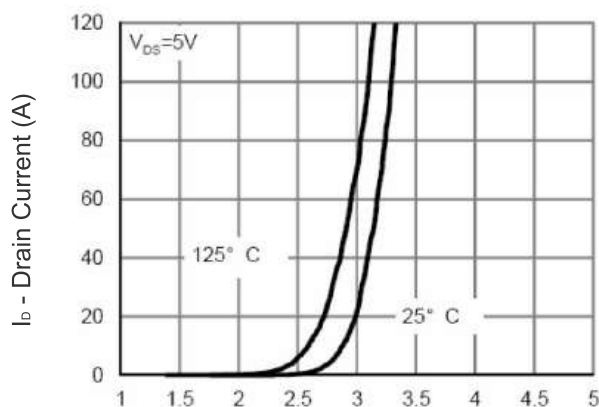
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



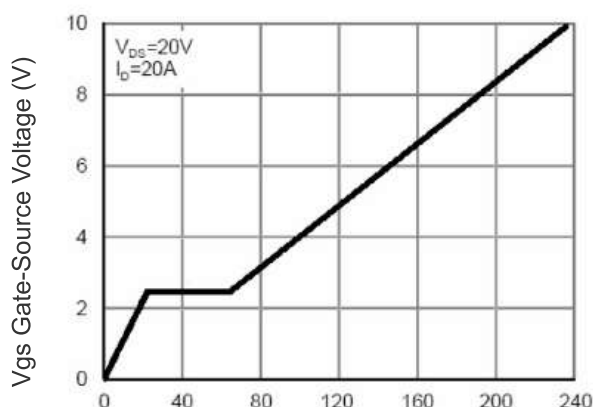
Tj -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



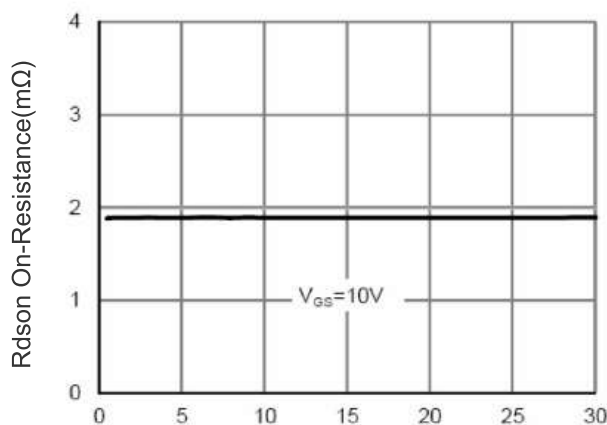
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



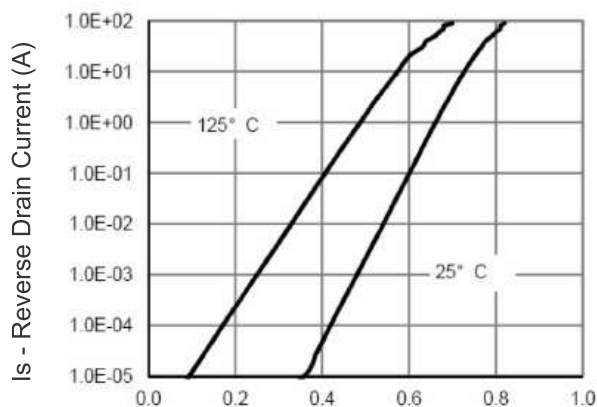
Qg Gate Charge (nC)

Figure 5 Gate Charge



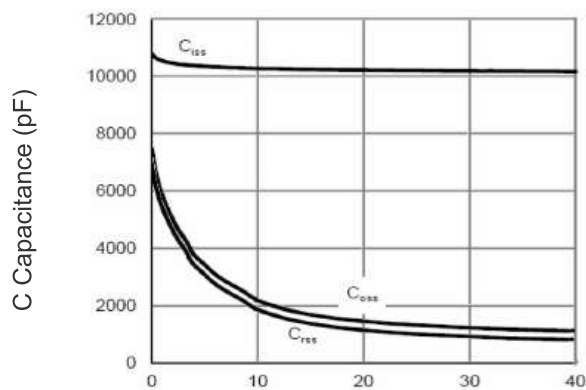
Id - Drain Current (A)

Figure 3 Rdson- Drain Current

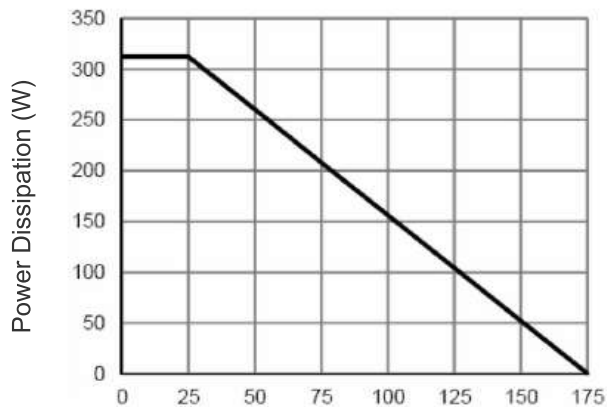


Vsd Source-Drain Voltage (V)

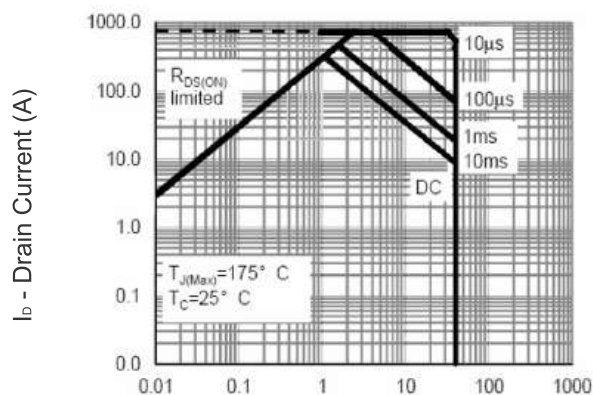
Figure 6 Source- Drain Diode Forward



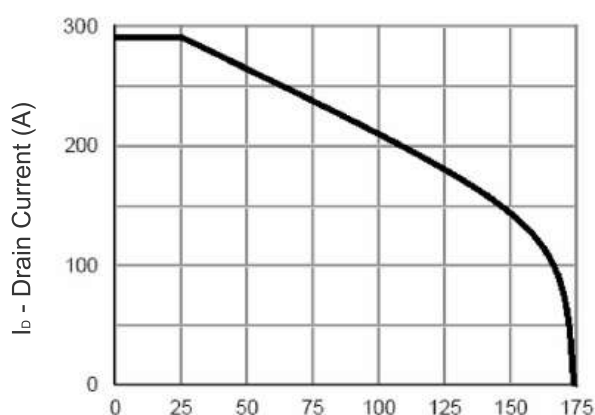
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



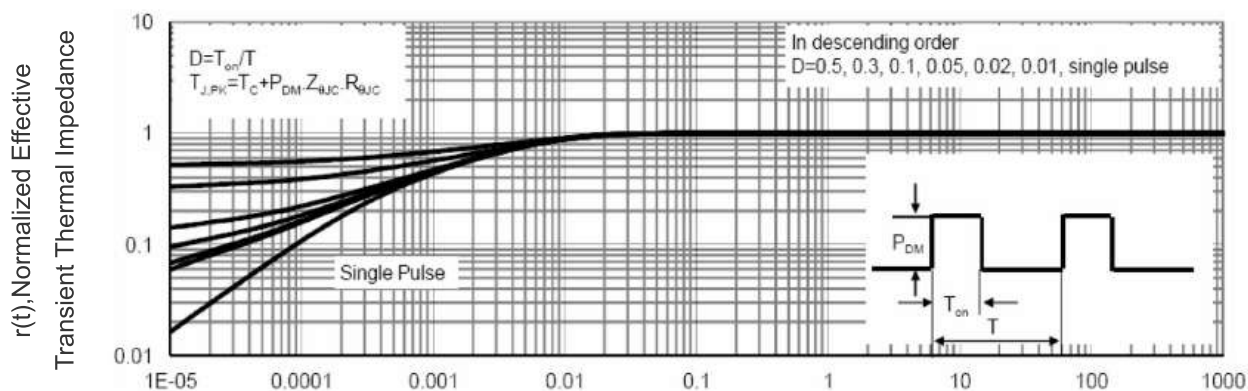
T_J -Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area

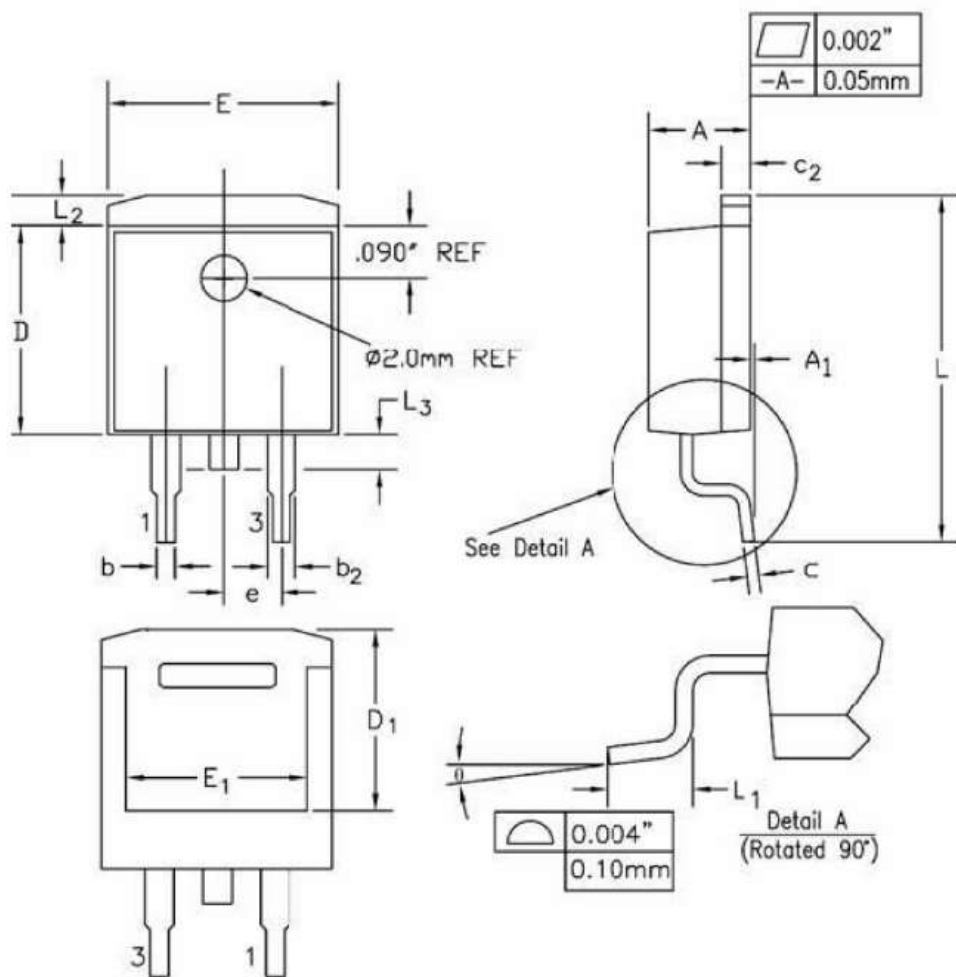


T_J -Junction Temperature(°C)
Figure 10 Current De-rating



Square Wave Pluse Duration(sec)
Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	
A1	-	0.010	-	0.25	
b	0.028	0.037	0.71	0.94	
b2	0.045	0.055	1.15	1.40	
c	0.018	0.024	0.46	0.61	
c2	0.048	0.055	1.22	1.40	
D	0.350	0.370	8.89	9.40	
D1	0.315	0.324	8.01	8.23	
E	0.395	0.405	10.04	10.28	
E1	0.310	0.318	7.88	8.08	
e	0.100 BSC.		2.54 BSC.		
L	0.580	0.620	14.73	15.75	
L1	0.090	0.110	2.29	2.79	
L2	0.045	0.055	1.15	1.39	
L3	0.050	0.070	1.27	1.77	
θ	0°	8°	0°	8°	

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