MJ N-Channel Enhancement Mode Power MOSFET

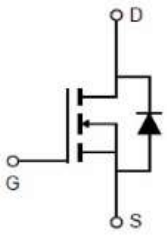
Description

The MJ4030K uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge .
The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

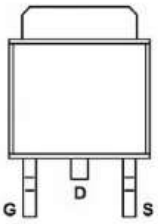
General Features

- N-Channel
  V_{DS} =40V,I_D =30A
  $R_{DS(ON)}$ <16mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <24mΩ @ V_{GS}=4.5V

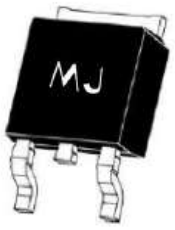
- High power and current handing capability
- Lead free product is acquired
- Surface mount package



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ4030K	MJ4030K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous(T_C =100℃)	$I_{D(100℃)}$	21.2	A
Pulsed Drain Current	I_{DM}	70	A
Maximum Power Dissipation	P_D	45	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	3.3	℃/W

N-CH Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=15A	-	12.3	16	mΩ
		V_{GS}=4.5V, I_D=15A	-	17	24	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=15A	-	15	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V F=1.0MHz	-	964	-	PF
Output Capacitance	C_{oss}		-	109	-	PF
Reverse Transfer Capacitance	C_{rss}		-	96	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V, R_L=1.3Ω V_{GS}=10V,R_{GEN}=3Ω	-	5.5	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=15A V_{GS}=10V	-	22.9	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	5.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=15A	-	0.8	1.2	V

N- Channel Typical Electrical and Thermal Characteristics (Curves)

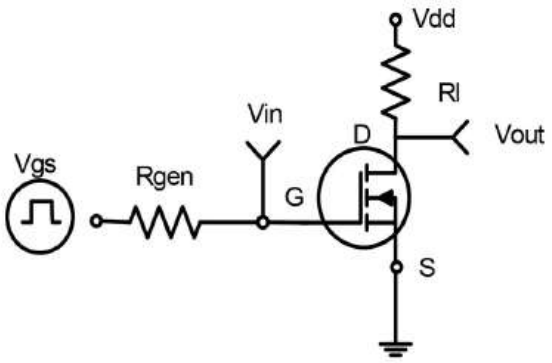


Figure 1 Switching Test Circuit

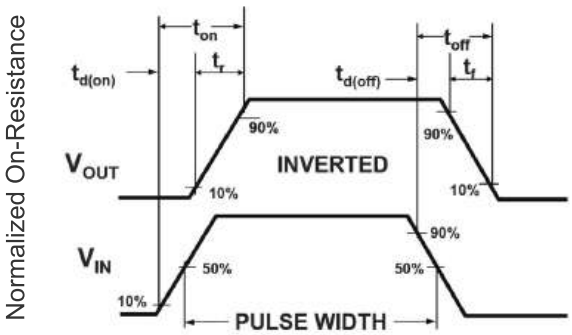


Figure 2 Switching Waveforms

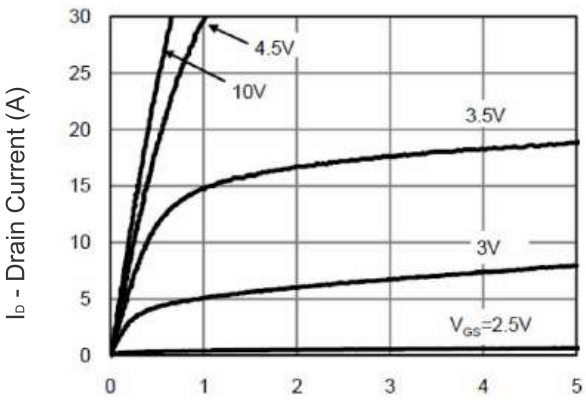


Figure 3 Output Characteristics

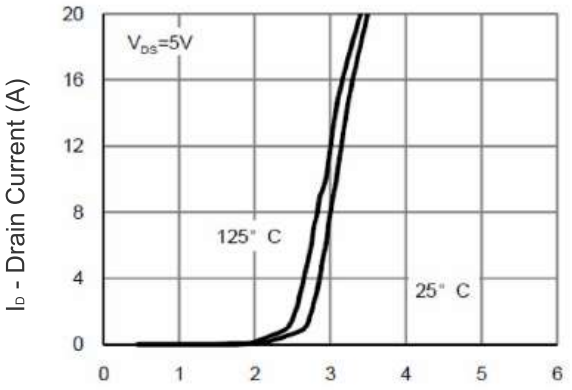


Figure 4 Transfer Characteristics

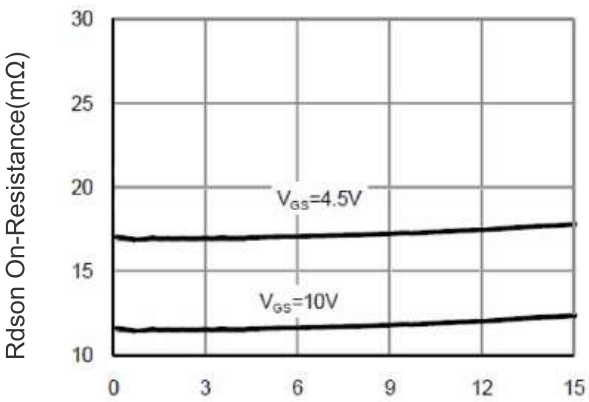


Figure 5 Drain-Source On-Resistance

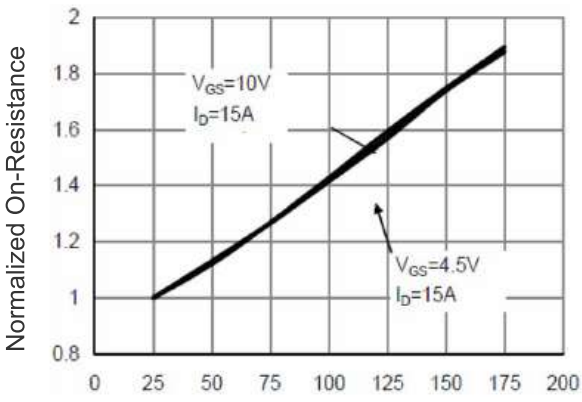
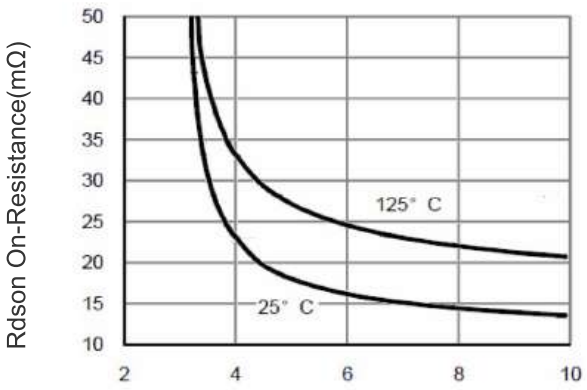
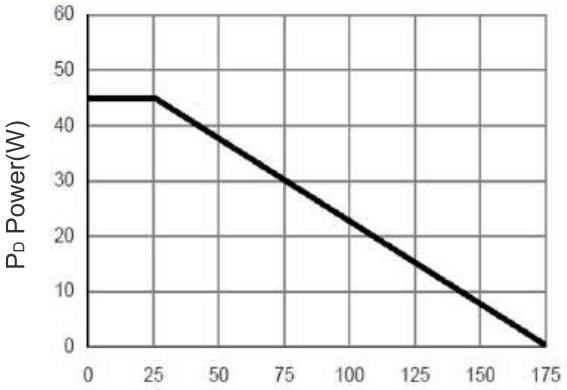


Figure 6 Drain-Source On-Resistance



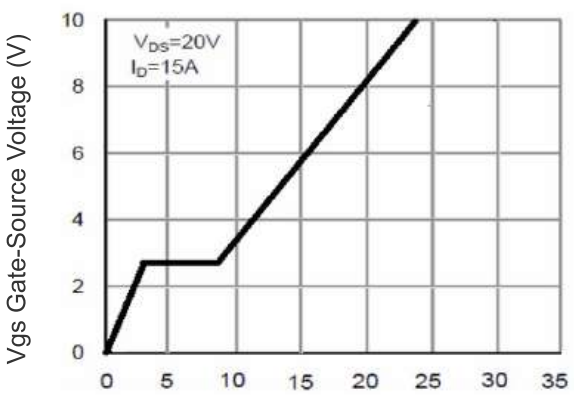
Vgs Gate-Source Voltage (V)

Figure7 Rdson vs Vgs



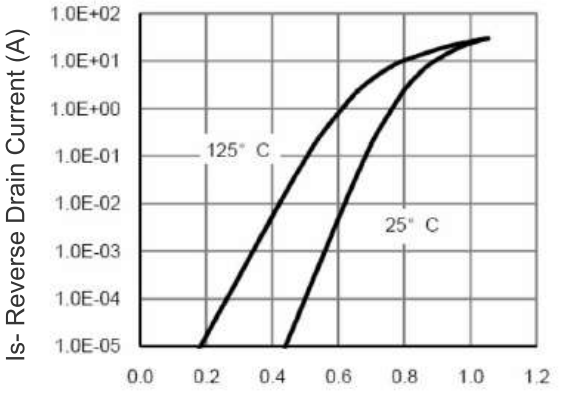
TJ-Junction Temperature(℃)

Figure 8 Power Dissipation



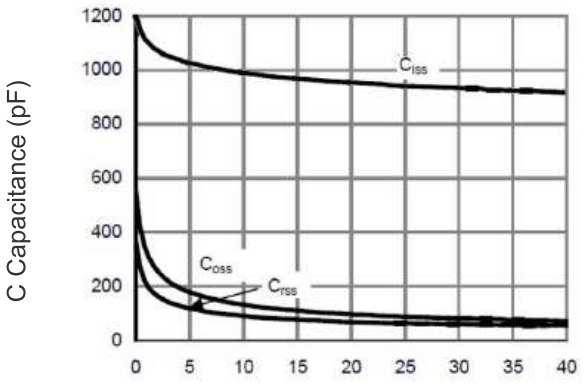
Qg Gate Charge (nC)

Figure 9 Gate Charge



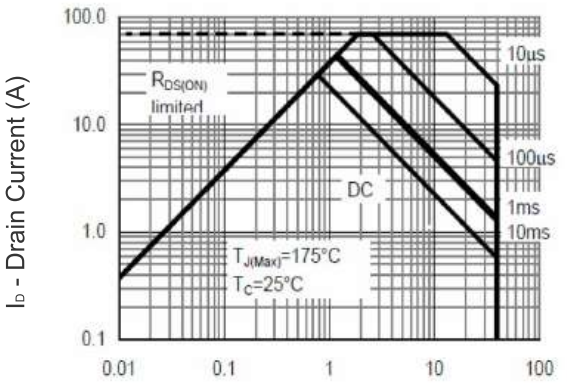
Vds Drain-Source Voltage (V)

Figure 10 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)

Figure 11 Capacitance vs Vds



Vds Drain-Source Voltage (V)

Figure 12 Safe Operation Area

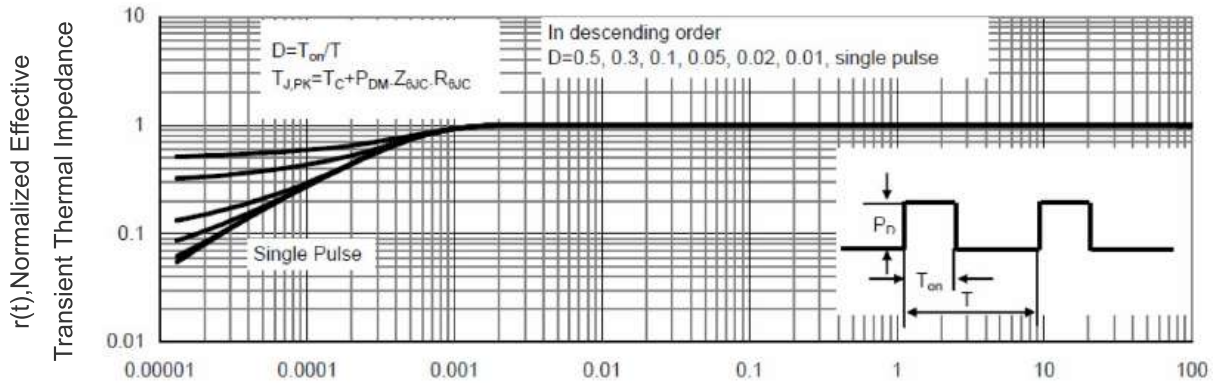
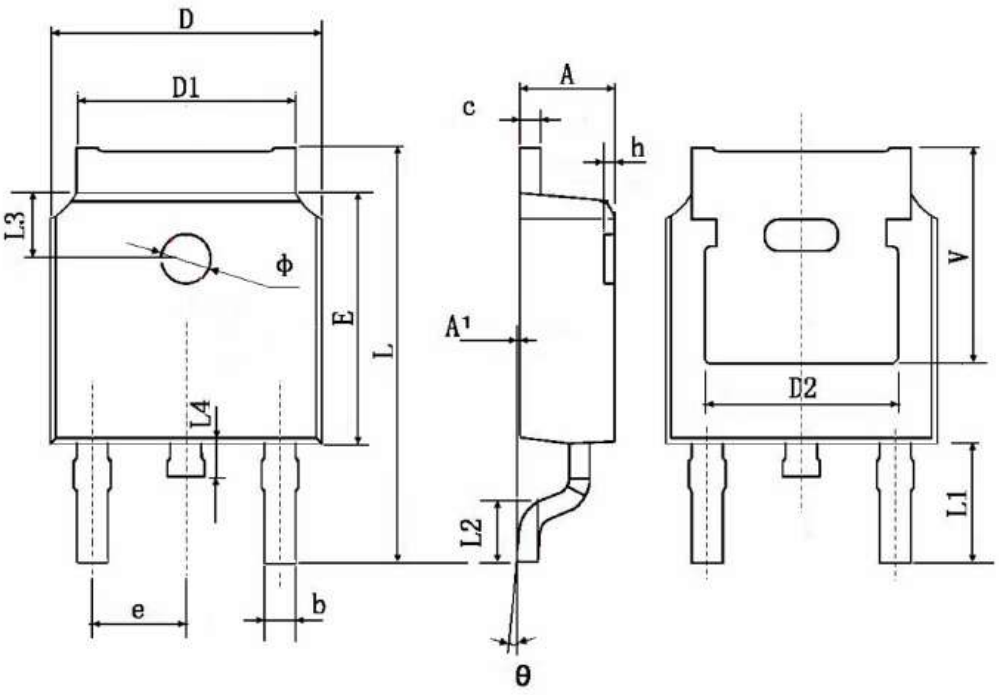


Figure 13 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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