MJ N-Channel Enhancement Mode Power MOSFET

Description

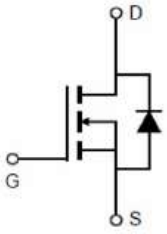
The MJ33H29D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- V_{DS} =33V,I_D =290A
  $R_{DS(ON)}$ <1.8mΩ @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply



Schematic diagram

TO-263-2L top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ33H29D	MJ33H29D	TO-263-2L	-	-	-

Absolute Maximum Ratings (T_A =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	33	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	290	A
Drain Current-Continuous(T_C=100℃)	$I_{D(100℃)}$	205	A
Pulsed Drain Current	I_{DM}	1160	A
Maximum Power Dissipation	P_D	270	W
Derating factor		1.8	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	1300	mJ
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.56	℃/W

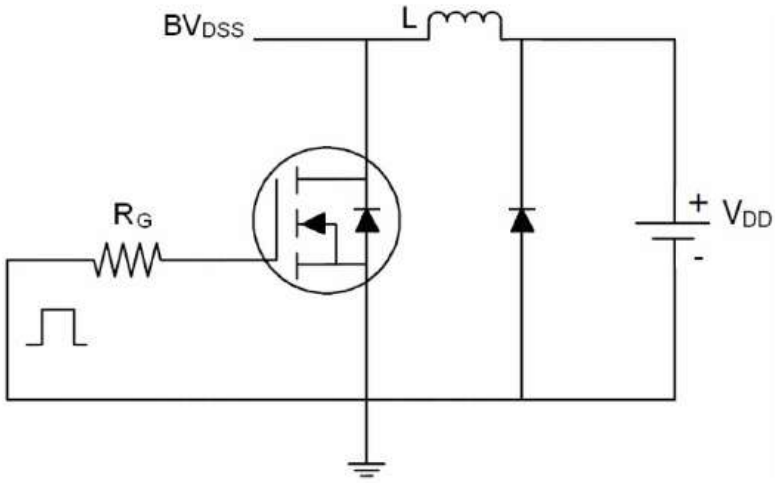
Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	33	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=33V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=160A	-	1.4	1.8	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=160A	50	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V F=1.0MHz	-	7848	-	PF
Output Capacitance	C_{oss}		-	2046	-	PF
Reverse Transfer Capacitance	C_{rss}		-	1516	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,R_L=15Ω R_G=2.5Ω,V_{GS}=10V	-	17	-	nS
Turn-on Rise Time	t_r		-	160	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	80	-	nS
Turn-Off Fall Time	t_f		-	100	-	nS
Total Gate Charge	Q_g	I_D=160A,V_{DD}=15V V_{GS}=10V	-	168	-	nC
Gate-Source Charge	Q_{gs}		-	32.5	-	nC
Gate-Drain Charge	Q_{gd}		-	72.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=160A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	290	A
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=160A di/dt=100A/μs (Note 3)	-	45	-	nS
Reverse Recovery Charge	Q_{rr}		-	160	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

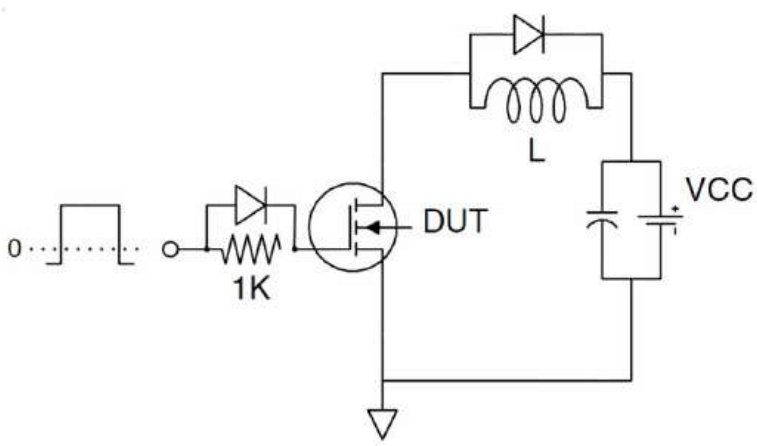
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,Rg=25Ω

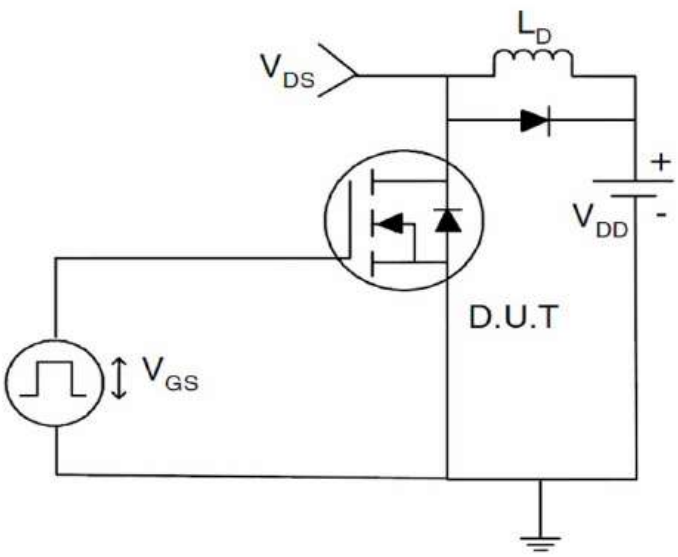
Test circuit



EAS test Circuit



Gate charge test Circuit



Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)

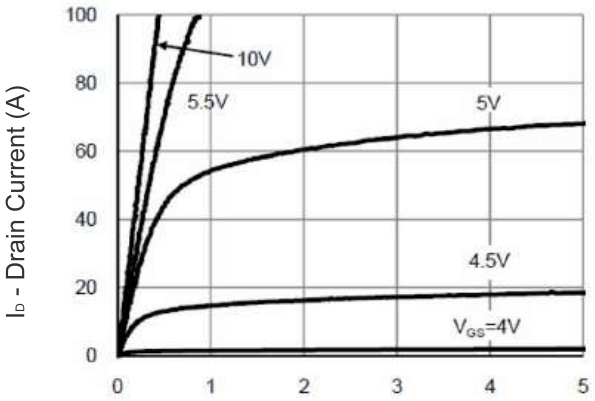


Figure 1 Output Characteristics

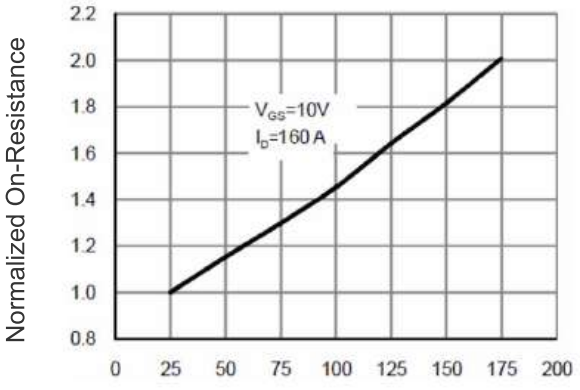


Figure 4 Rdson-Junction Temperature

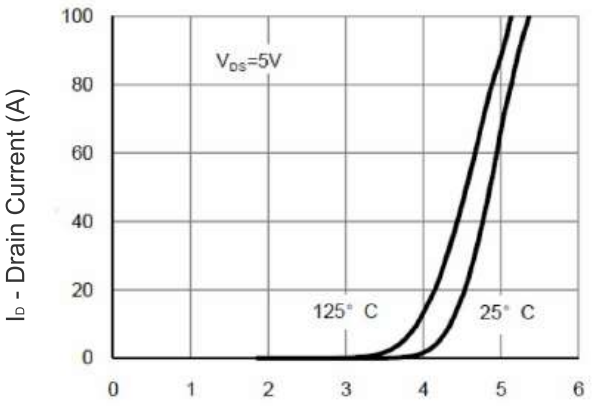


Figure 2 Transfer Characteristics

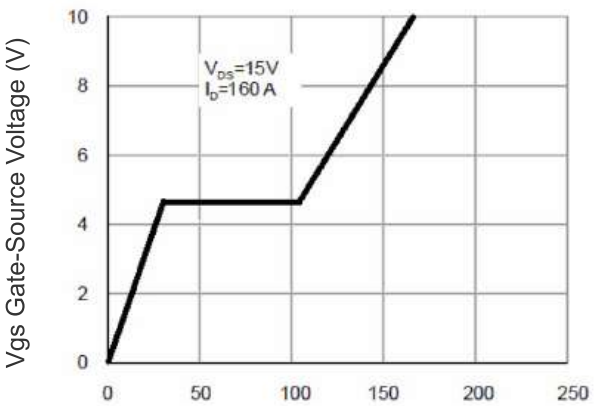


Figure 5 Gate Charge

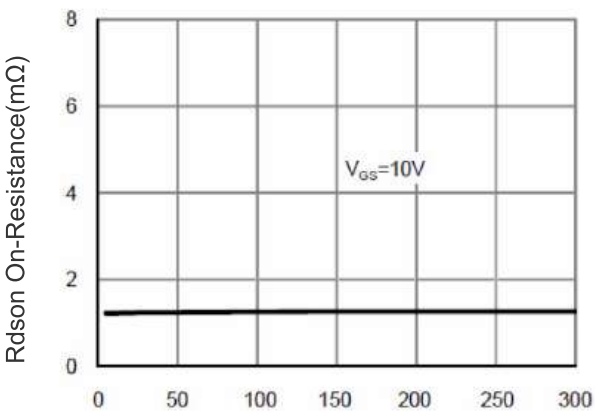


Figure 3 Rdson- Drain Current

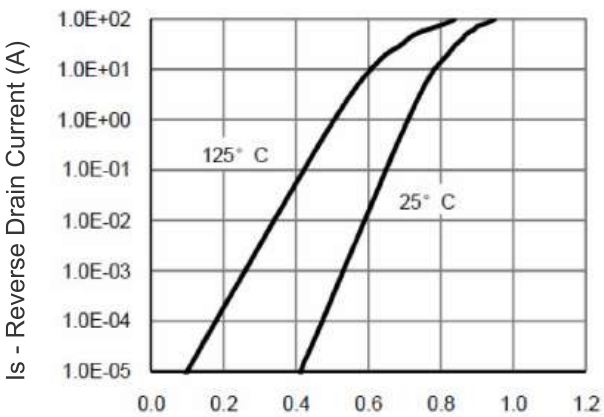
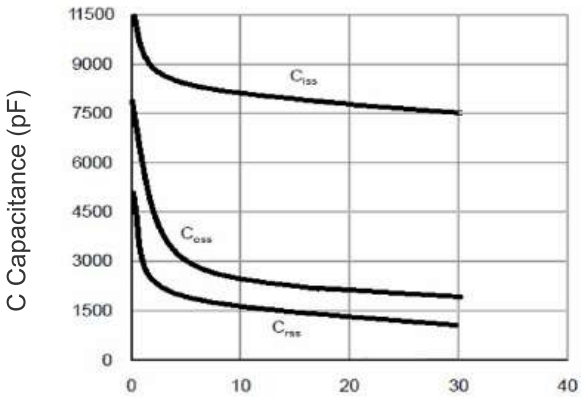
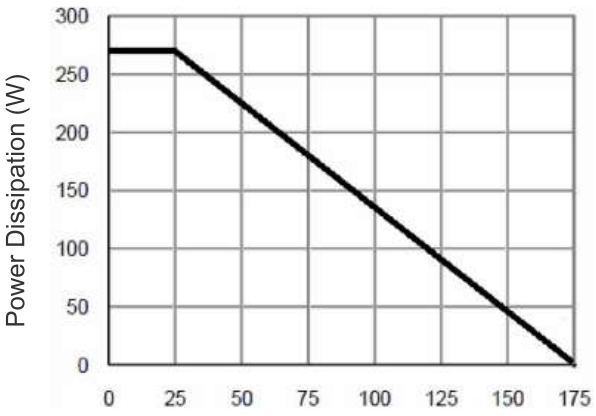


Figure 6 Source- Drain Diode Forward



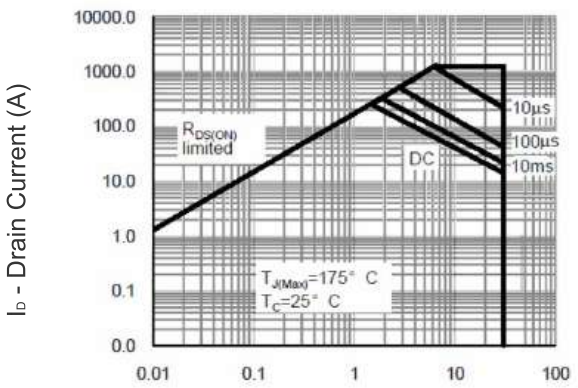
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



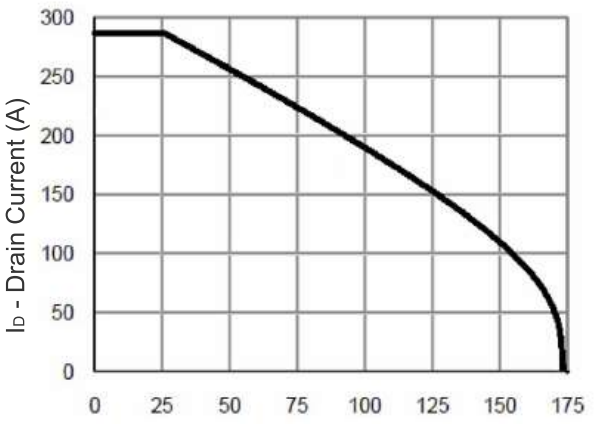
TJ -Junction Temperature(℃)

Figure 9 Power De-rating



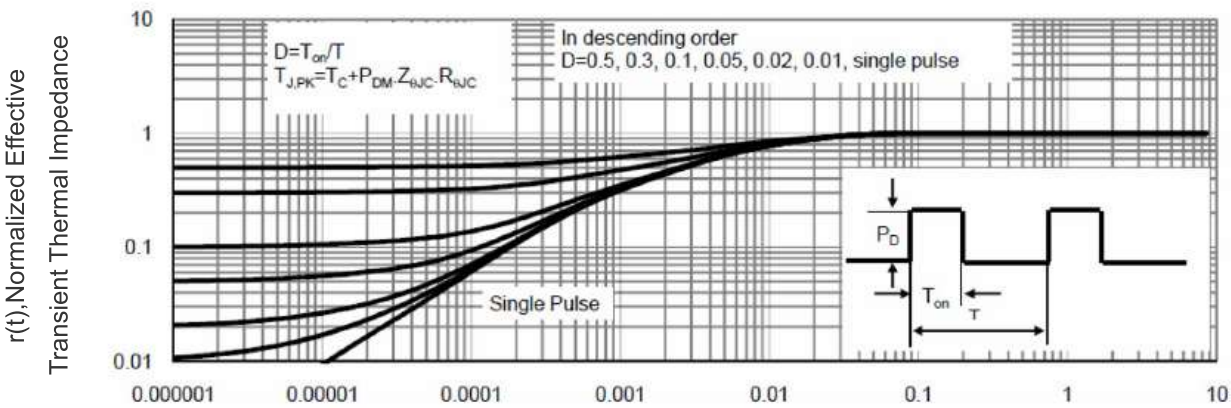
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ -Junction Temperature(℃)

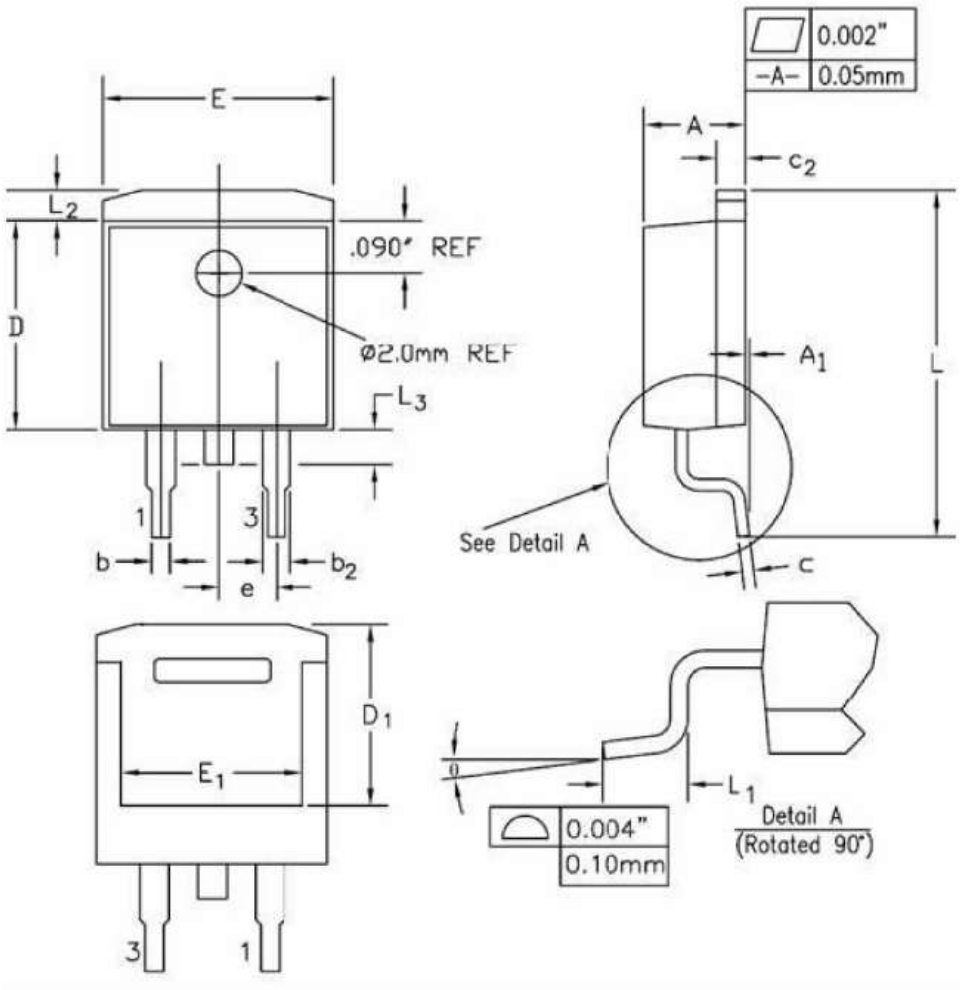
Figure 10 Current vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	
A1	-	0.010	-	0.25	
b	0.028	0.037	0.71	0.94	
b2	0.045	0.055	1.15	1.40	
c	0.018	0.024	0.46	0.61	
c2	0.048	0.055	1.22	1.40	
D	0.350	0.370	8.89	9.40	
D1	0.315	0.324	8.01	8.23	
E	0.395	0.405	10.04	10.28	
E1	0.310	0.318	7.88	8.08	
e	0.100 BSC.		2.54 BSC.		
L	0.580	0.620	14.73	15.75	
L1	0.090	0.110	2.29	2.79	
L2	0.045	0.055	1.15	1.39	
L3	0.050	0.070	1.27	1.77	
θ	0°	8°	0°	8°	

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