MJ P-Channel Enhancement Mode Power MOSFET

Description

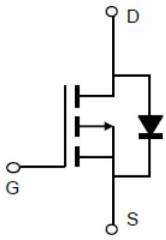
The MJ30P25Q uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge.
This device is suitable for use as a load switch or in PWM applications.

General Features

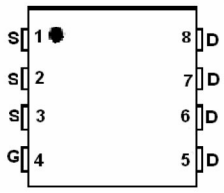
- ◆ V_{DS}=-30V,I_D=-25A
  $R_{DS(ON)}$<20mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$<11mΩ @ V_{GS}=-10V
- ◆ High Power and current handing capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

Application

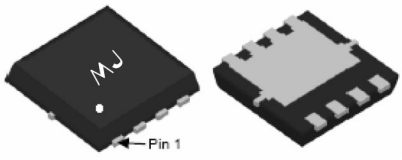
- ◆ PWM applications
- ◆ Load switch
- ◆ Power management



Schematic diagram



pin assignment



Top View Bottom View

100% UIS TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ30P25Q	MJ30P25Q	DFN3.3X3.3-8L	Ø330mm	12mm	5000 units

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-25	A
Drain Current-Continuous(T_C =100℃)	$I_{D(100℃)}$	-17.7	A
Drain Current-Pulsed (Note 1)	I_{DM}	-100	A
Maximum Power Dissipation	P_D	40	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JA}$	3.13	℃/W

Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=-250μA	-1	-1.7	-2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-15A	-	8.9	11	mΩ
		V_{GS}=-4.5V, I_D=-15A	-	15	20	mΩ
Gate resistance	R_G		-	5.2	-	Ω
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-15A	15	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	1632	-	PF
Output Capacitance	C_{oss}		-	227	-	PF
Reverse Transfer Capacitance	C_{rss}		-	178	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V, I_D=-15A, V_{GS}=-10V,R_{GEN}=1Ω	-	12	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	nS
Turn-Off Fall Time	t_f		-	13	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-20A, V_{GS}=-10V	-	45.6	-	nC
Gate-Source Charge	Q_{gs}		-	4.6	-	nC
Gate-Drain Charge	Q_{gd}		-	11.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-15A	-		-1.2	V

Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

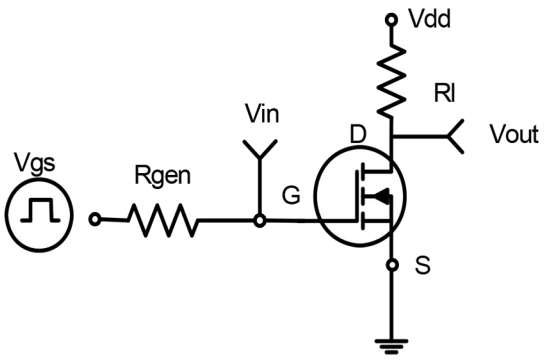


Figure 1 Switching Test Circuit

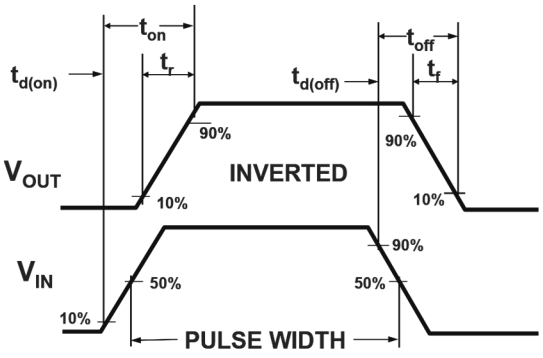


Figure 2 Switching Waveforms

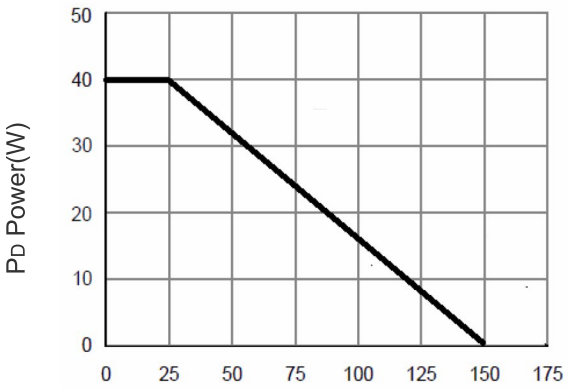


Figure 3 Power Dissipation

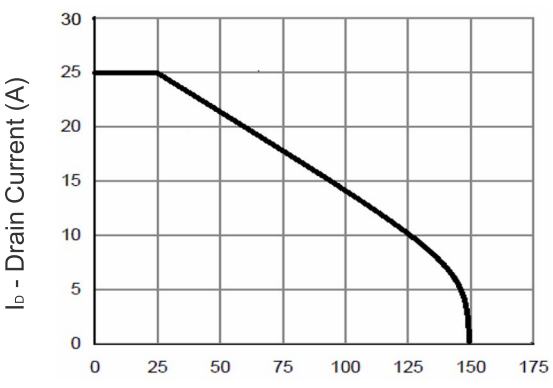


Figure 4 Drain Current

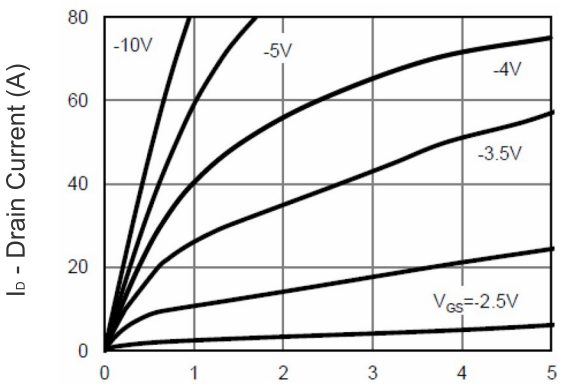


Figure 5 Output Characteristics

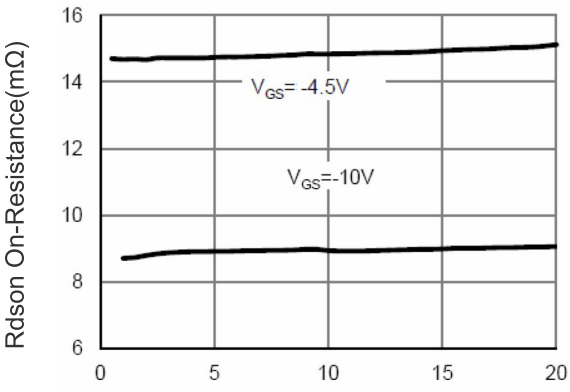


Figure 6 Drain-Source On-Resistance

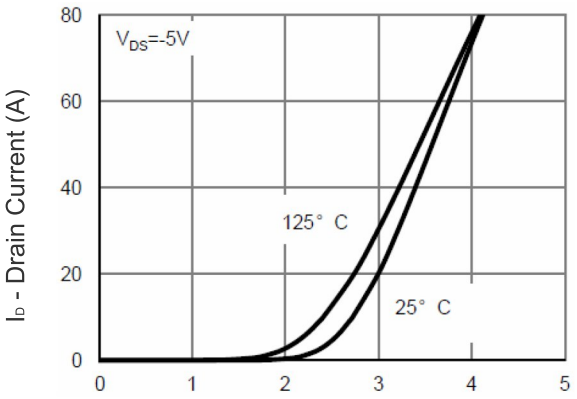


Figure 7 Transfer Characteristics

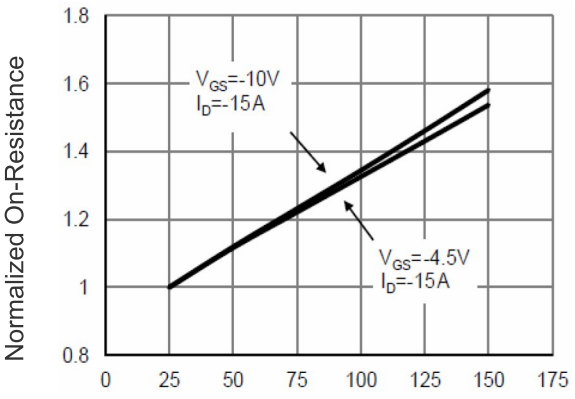


Figure 8 Drain-Source On-Resistance

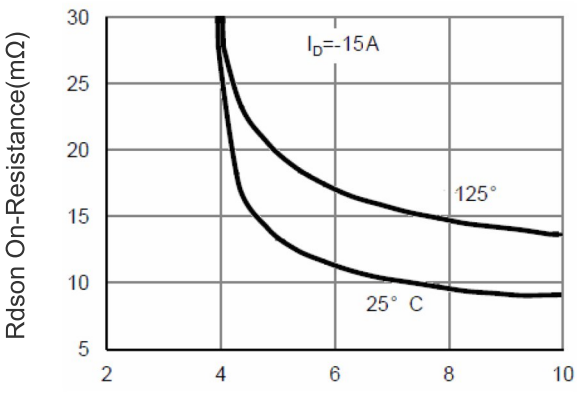


Figure 9 Rdson vs Vgs

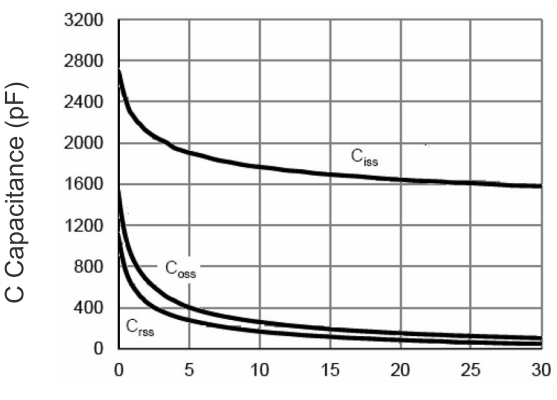


Figure 10 Capacitance vs Vds

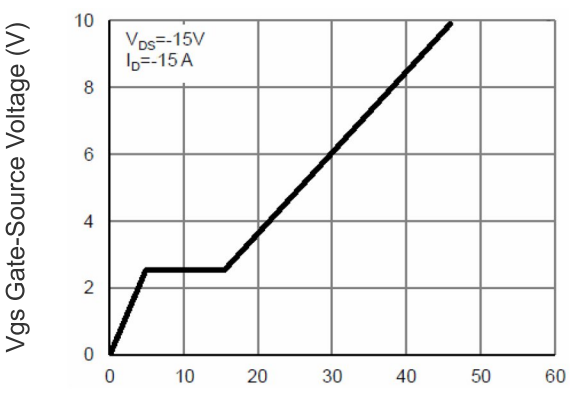


Figure 11 Gate Charge

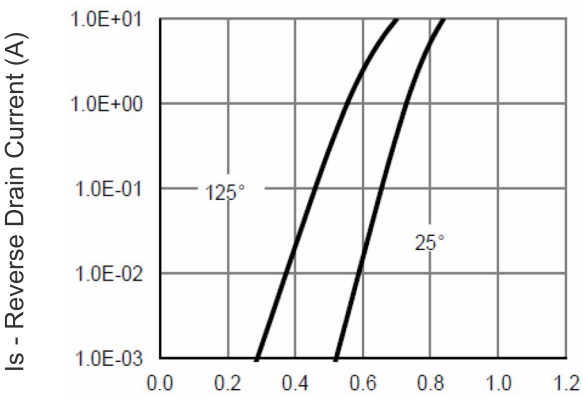


Figure 12 Source- Drain Diode Forward

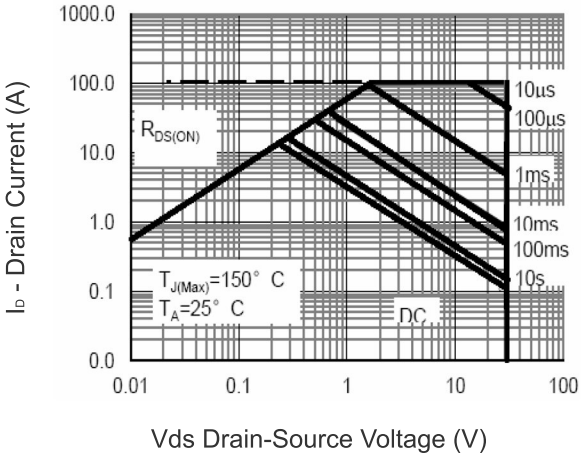


Figure 13 Safe Operation Area

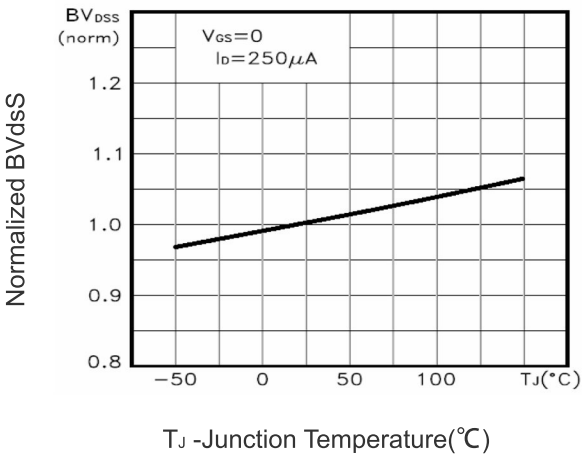


Figure 14 BV_{DSS} vs Junction Temperature

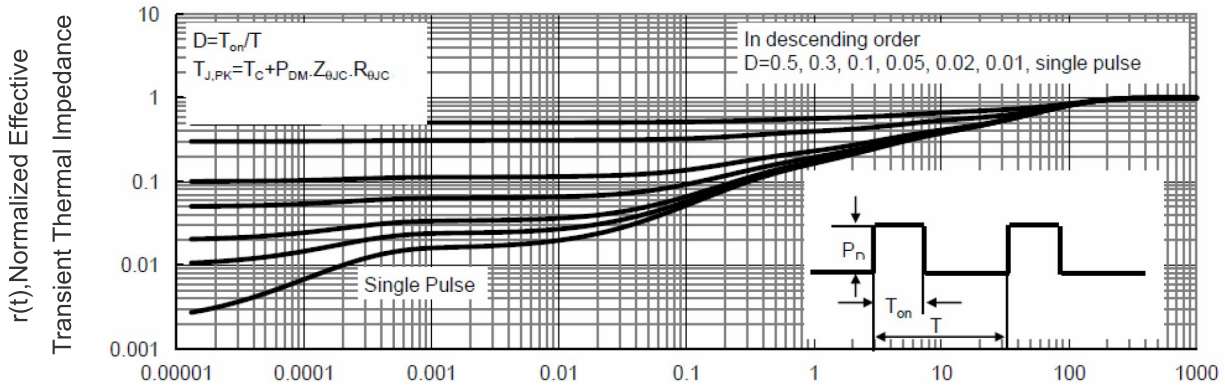
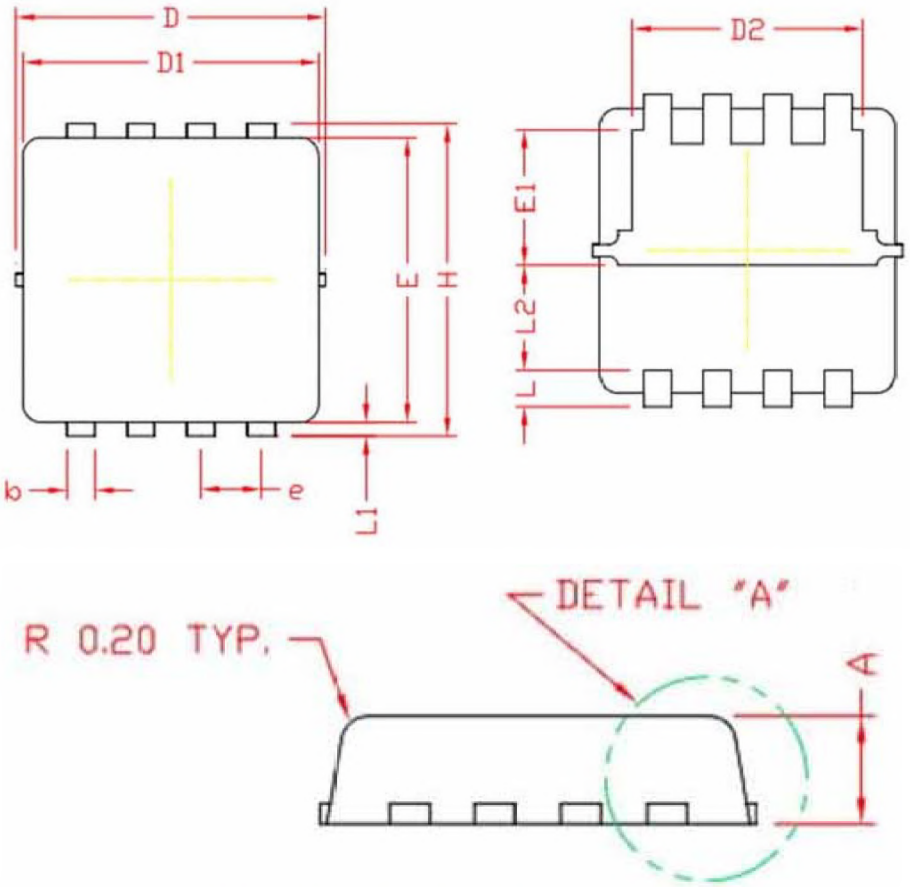


Figure 15 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information



(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.80	0.90
A1	0.00	0.03	0.05
b	0.24	0.30	0.35
c	0.10	0.15	0.20
D	3.25	3.32	3.40
D1	3.05	3.15	3.25
D2	2.40	2.50	2.60
E	3.00	3.10	3.20
E1	1.35	1.45	1.55
e	0.65 BSC.		
H	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.10	0.15	0.20
L2	1.13 REF.		

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