

MJ N-Channel Enhancement Mode Power MOSFET

Description

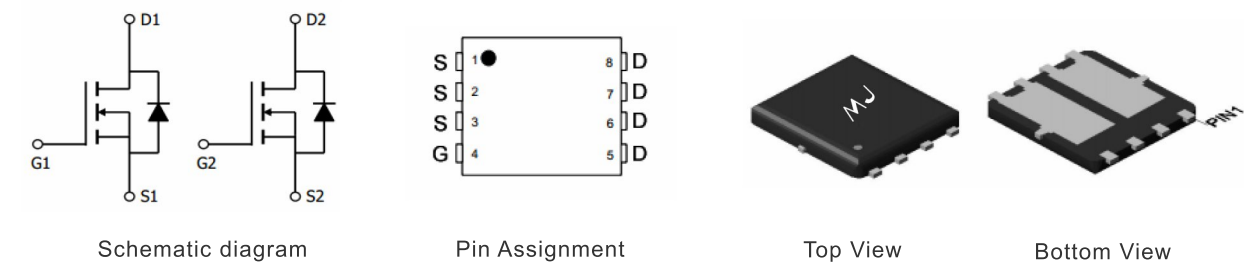
The MJ30ND35Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- ◆ $V_{DS}=30V, I_D=35A$
 $R_{DS(ON)}<13m\Omega$ @ $V_{GS}=10V$
 $R_{DS(ON)}<19m\Omega$ @ $V_{GS}=4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized Avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

- ◆ Power switching application
- ◆ Hard Switched and High Frequency Circuits
- ◆ Uninterruptible Power Supply



100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ30ND35Q	MJ30ND35Q	DFN 3.3x3.3-8L	-	-	-

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	35	A
Drain Current-Continuous($T_C=100^{\circ}C$)	$I_{D(100^{\circ}C)}$	24.8	A
Pulsed Drain Current	I_{DM}	140	A
Maximum Power Dissipation	P_D	30	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	0.24	mJ
Derating factor		72	W/°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JA}$	4.17	°C/W
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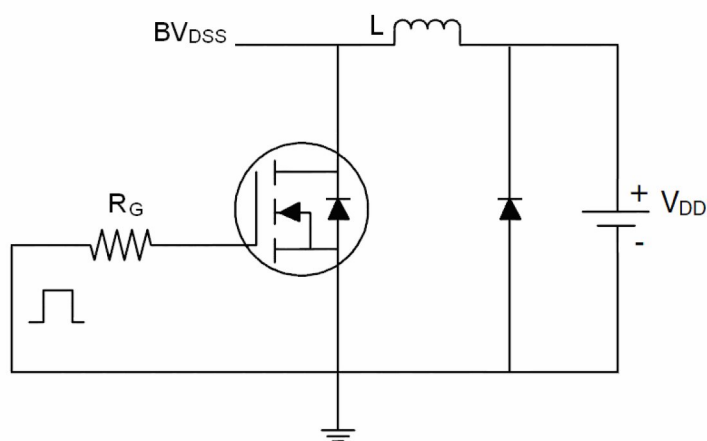
Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	0.9	1.3	2.0	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	11	13	mΩ
		V _{GS} =4.5V, I _D =20A	-	14.5	19	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =20A	26	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =15V,V _{GS} =0V, F=1.0MHz	-	1000	-	PF
Output Capacitance	C _{oss}		-	180.8	-	PF
Reverse Transfer Capacitance	C _{rss}		-	164.4	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, R _L =0.75Ω V _{GS} =10V,R _G =3Ω	-	5	-	nS
Turn-on Rise Time	t _r		-	12	-	nS
Turn-Off Delay Time	t _{d(off)}		-	19	-	nS
Turn-Off Fall Time	t _f		-	6	-	nS
Total Gate Charge	Q _g	V _{DS} =15V,I _D =20A, V _{GS} =10V	-	17	-	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	nC
Gate-Drain Charge	Q _{gd}		-	3.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =-20A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	35	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =20A di/dt=100A/μs ^(Note 3)	-	19	-	nS
Reverse Recovery Charge	Q _{rr}		-	10	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

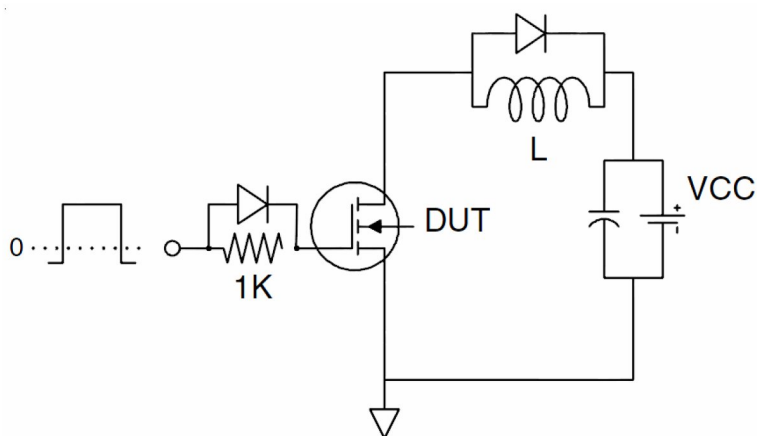
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C,V_{DD}=15V,V_G=10V,L=0.5mH,R_G=25Ω

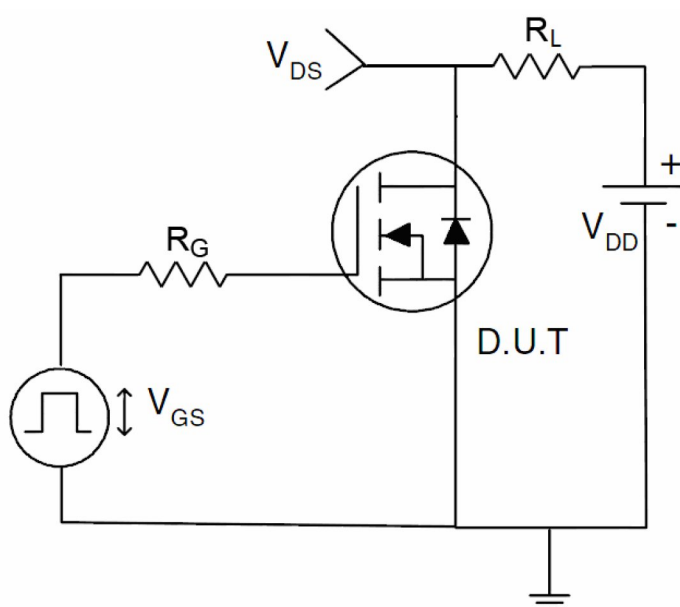
Test circuit



EAS test Circuit

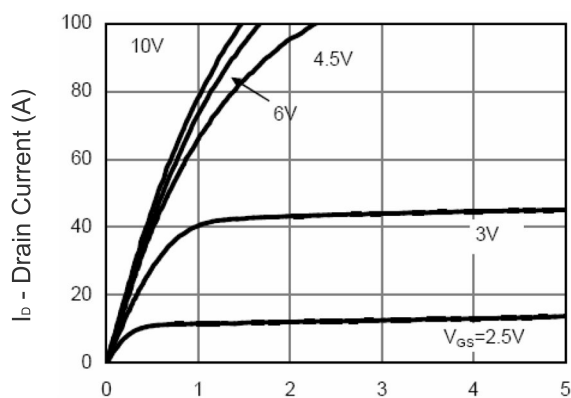


Gate charge test Circuit



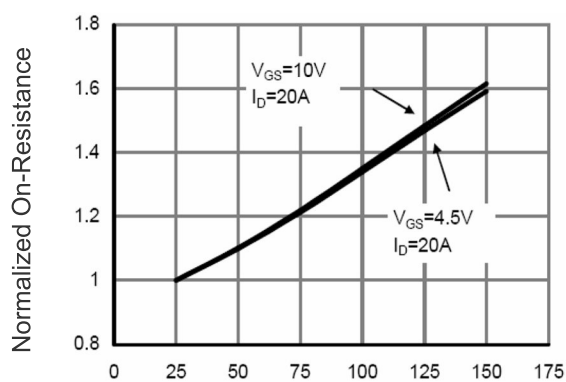
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



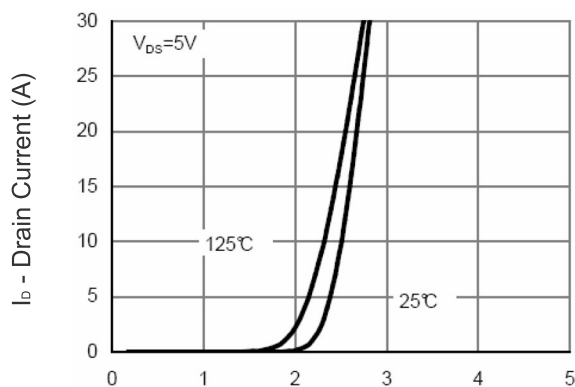
V_{ds} Drain-Source Voltage (V)

Figure 1 Output Characteristics



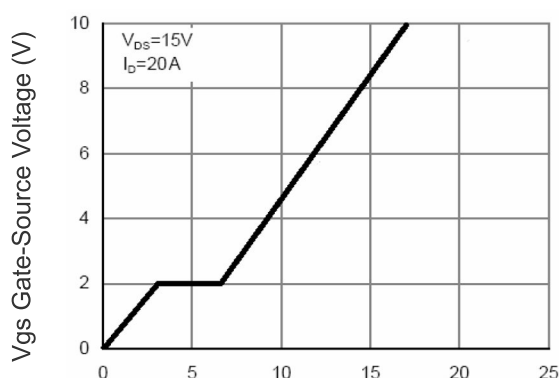
T_J -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



V_{gs} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



Q_g Gate Charge (nC)

Figure 5 Gate Charge

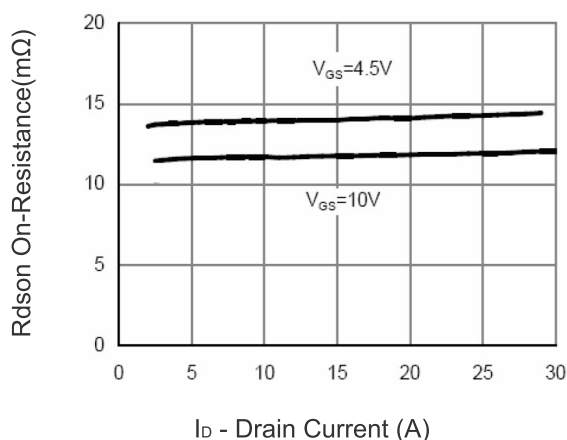


Figure 3 Rdson- Drain Current

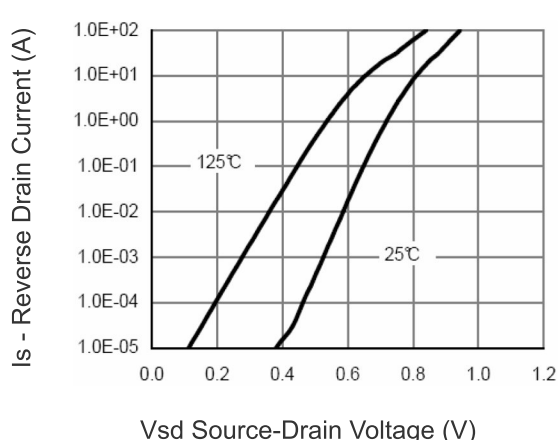
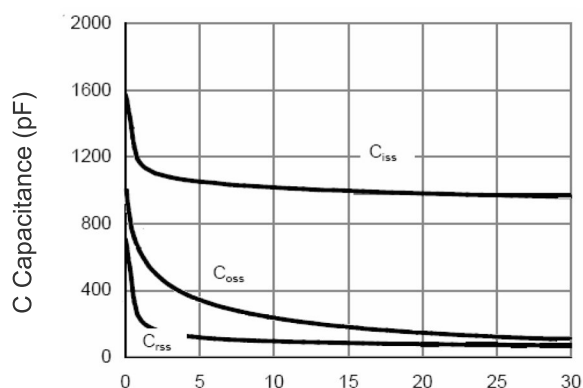
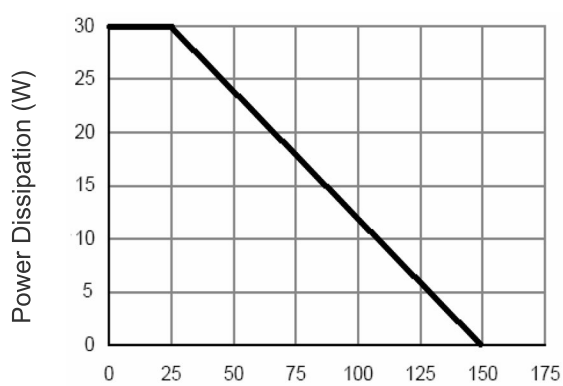


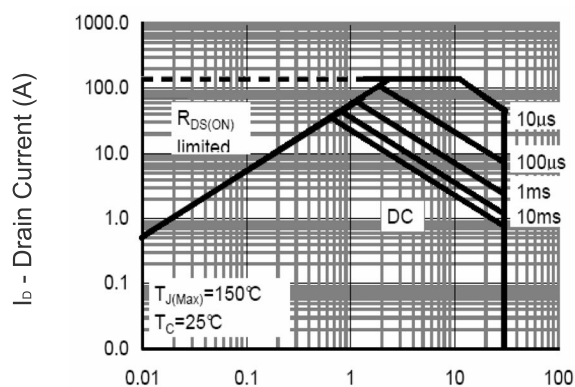
Figure 6 Source- Drain Diode Forward



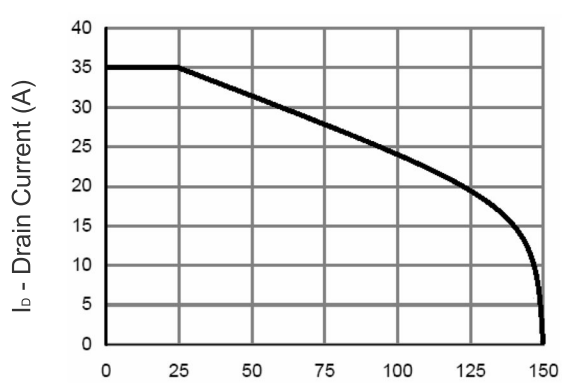
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



TJ -Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



TJ -Junction Temperature(°C)
Figure 10 Id Current De-rating

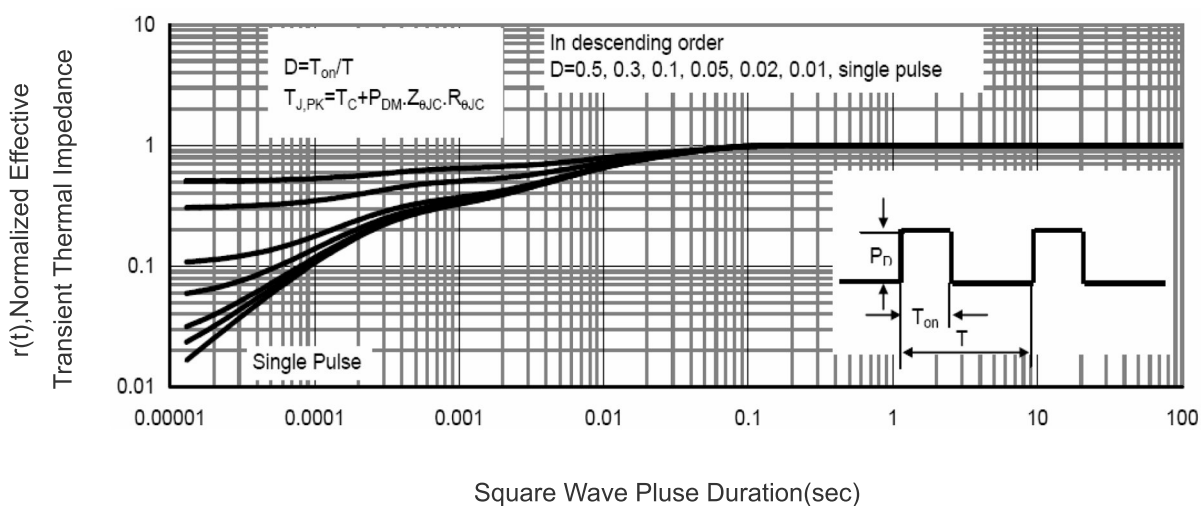
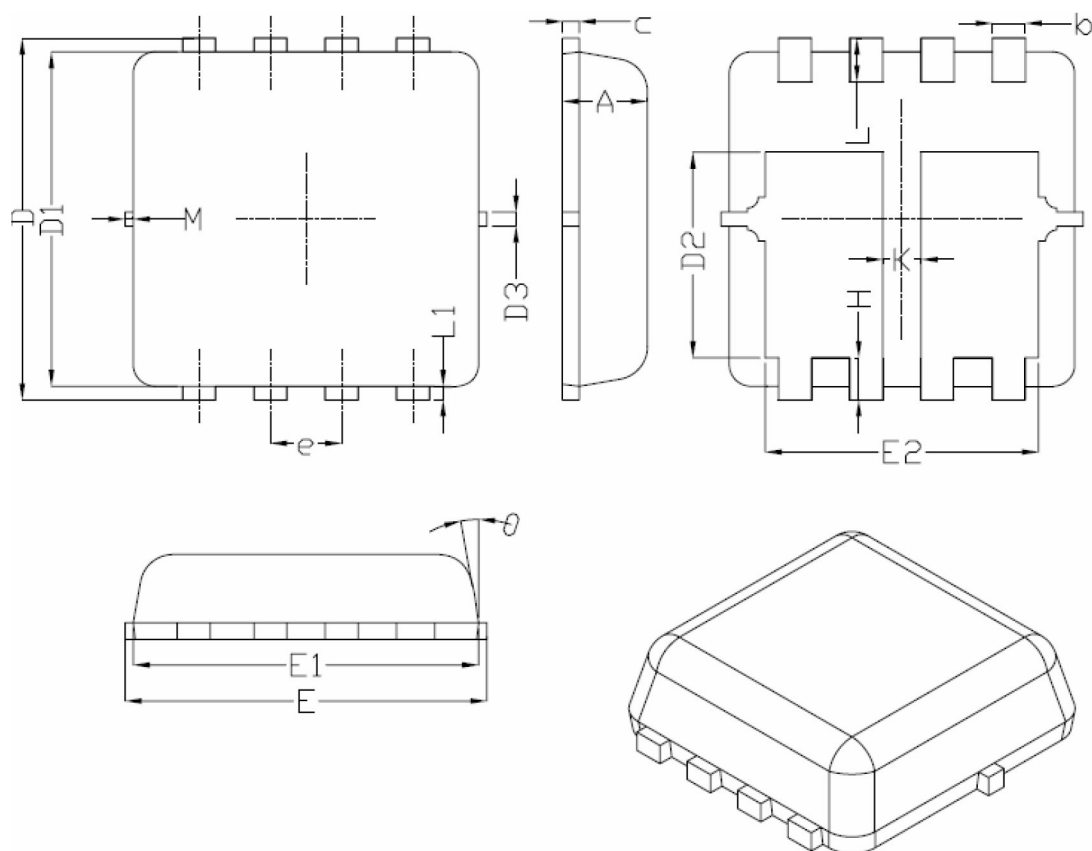


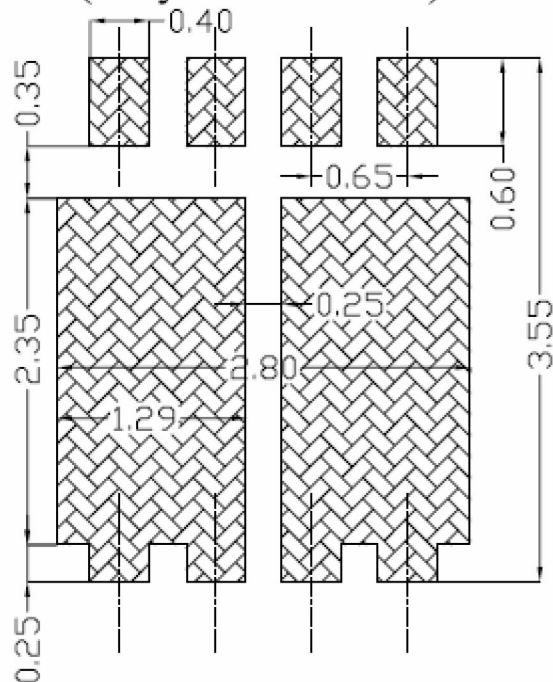
Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information



Land Pattern
(Only for Reference)

SYMBOL	DIMENSIONAL REOMTS		
	MIN	NOM	MAX
<i>A</i>	0.70	0.75	0.80
<i>b</i>	0.25	0.30	0.35
<i>c</i>	0.10	0.15	0.25
<i>D</i>	3.25	3.35	3.45
<i>D1</i>	3.00	3.10	3.20
<i>D2</i>	1.78	1.88	1.98
<i>D3</i>	---	0.13	---
<i>E</i>	3.20	3.30	3.40
<i>E1</i>	3.00	3.15	3.20
<i>E2</i>	2.39	2.49	2.59
<i>e</i>	0.65BSC		
<i>H</i>	0.30	0.39	0.50
<i>L</i>	0.30	0.40	0.50
<i>L1</i>	---	0.13	---
<i>K</i>	0.30	---	---
θ	---	10°	12°
<i>M</i>	*	*	0.15
* Not specified			



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