

MJ N-Channel Enhancement Mode Power MOSFET

Description

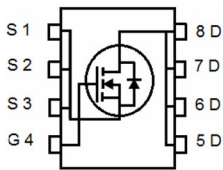
The MJ3065Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

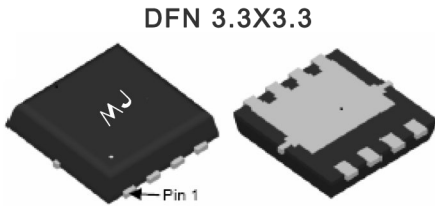
- ◆ $V_{DS}=30V, I_D=65A$
 $R_{DS(ON)}<4.5m\Omega$ (typical) @ $V_{GS}=10V$
 $R_{DS(ON)}<6.5m\Omega$ (typical) @ $V_{GS}=4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Very low on-resistance $R_{DS(on)}$
- ◆ Good stability and uniformity with high E_{AS}
- ◆ 150 °C operating temperature
- ◆ Pb-free lead plating

Application

- ◆ DC/DC Converter
- ◆ Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View

Bottom View

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ3065Q	MJ3065Q	DFN 3.3x3.3-8L	-	-	-

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Note 1)	I_D	65	A
Drain Current-Continuous($T_C =100^{\circ}C$)	$I_{D(100^{\circ}C)}$	46	A
Pulsed Drain Current	I_{DM}	260	A
Maximum Power Dissipation	P_D	45	W
Single pulse avalanche energy (Note 5)	E_{AS}	150	mJ
Derating factor		0.36	W/°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JA}$	2.8	°C/W
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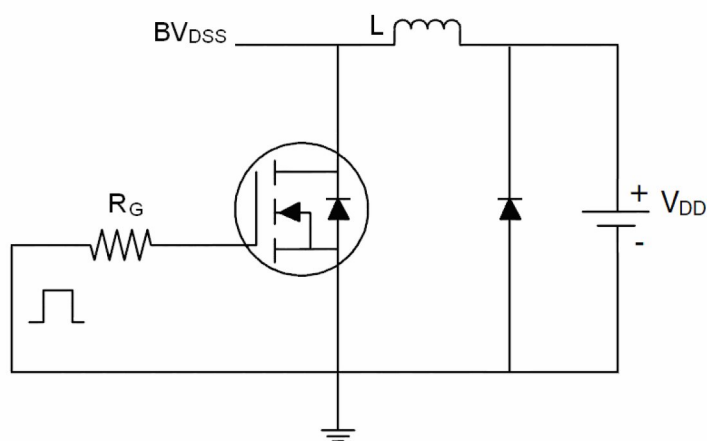
Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1	1.5	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	4.5	6.0	mΩ
		V _{GS} =4.5V, I _D =20A	-	6.5	8.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =20A	30	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =15V,V _{GS} =0V, F=1.0MHz	-	1784	-	PF
Output Capacitance	C _{oss}		-	266	-	PF
Reverse Transfer Capacitance	C _{rss}		-	212	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =5V,I _D =20A V _{GS} =10V,R _{GEN} =6Ω	-	7	-	nS
Turn-on Rise Time	t _r		-	6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	30	-	nS
Turn-Off Fall Time	t _f		-	8	-	nS
Total Gate Charge	Q _g	V _{DS} =15V,I _D =20A, V _{GS} =10V	-	38.4	-	nC
Gate-Source Charge	Q _{gs}		-	5.8	-	nC
Gate-Drain Charge	Q _{gd}		-	7.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =20A	-	0.85	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	65	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =20A di/dt=100A/μs ^(Note 3)	-	-	47	nS
Reverse Recovery Charge	Q _{rr}		-	-	25	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

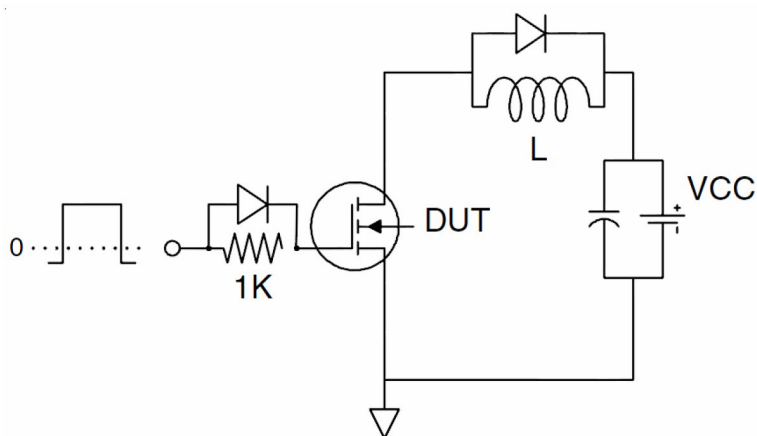
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C,V_{DD}=15V,V_G=10V,L=0.5mH,R_g=25Ω

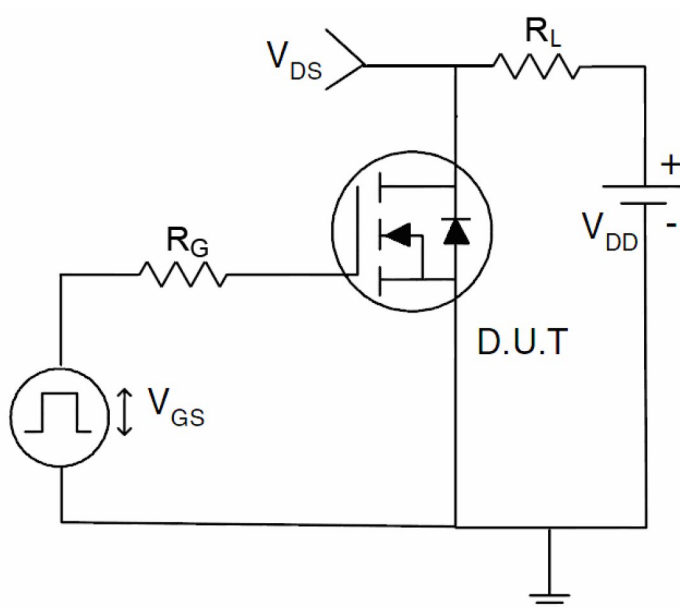
Test circuit



EAS test Circuit

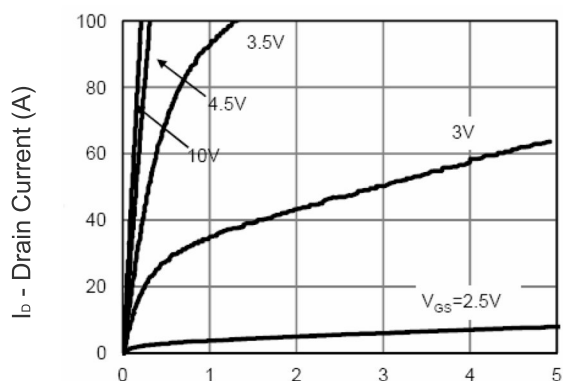


Gate charge test Circuit



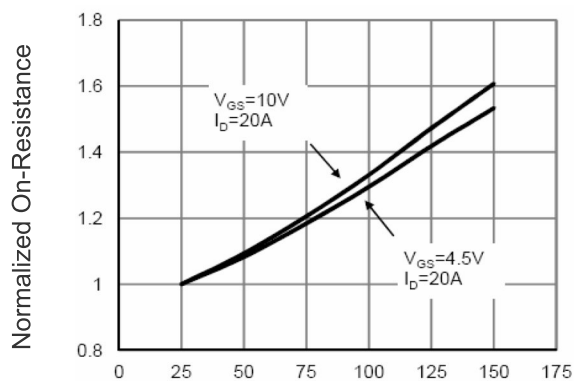
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



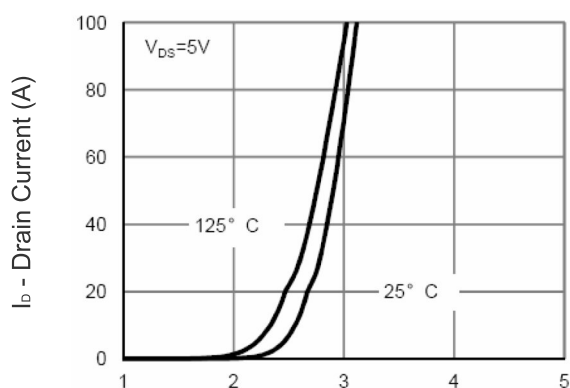
V_{ds} Drain-Source Voltage (V)

Figure 1 Output Characteristics



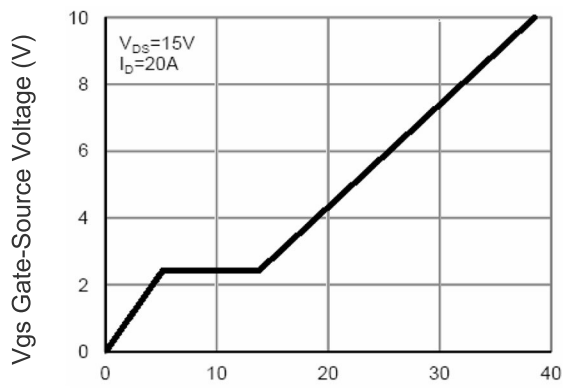
T_j -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



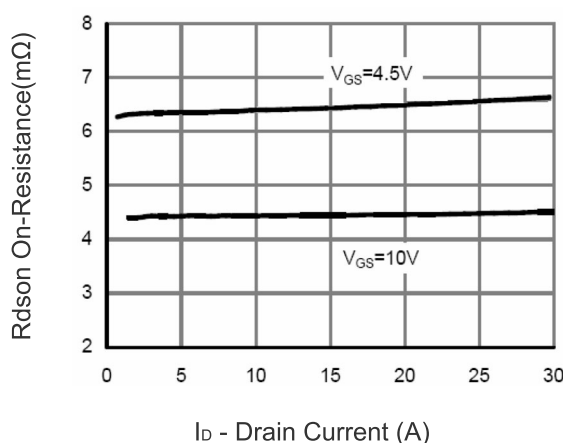
V_{gs} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



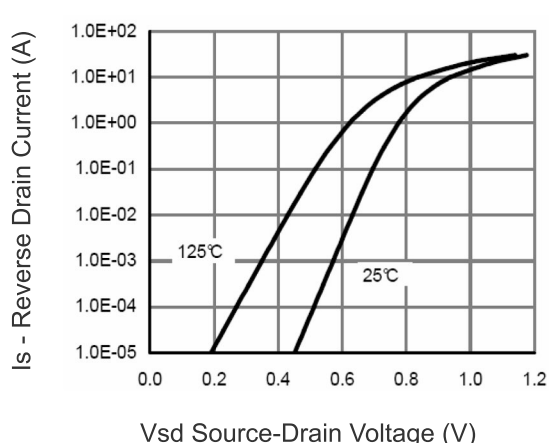
Q_g Gate Charge (nC)

Figure 5 Gate Charge



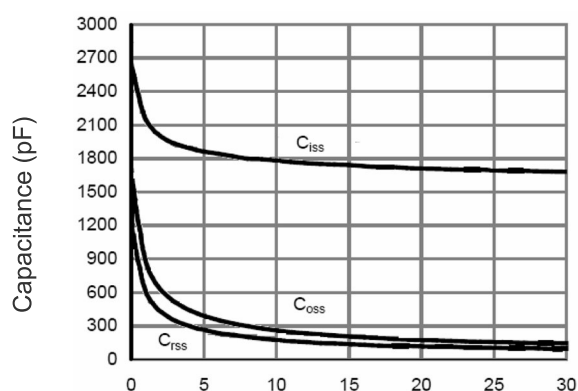
I_d - Drain Current (A)

Figure 3 Rdson- Drain Current



V_{sd} Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds

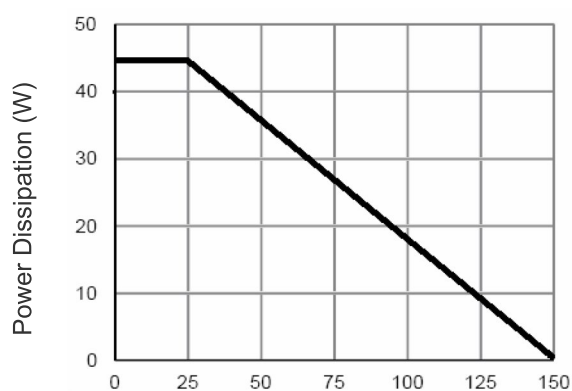
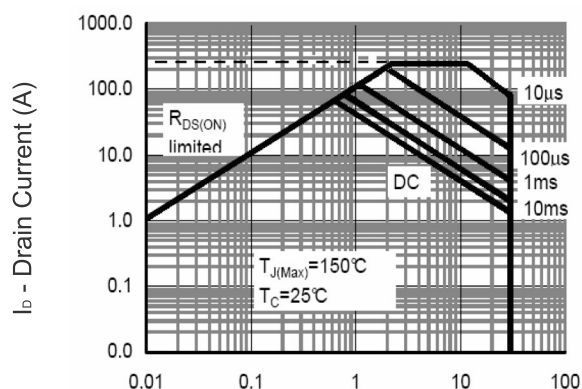

T_J -Junction Temperature(°C)

Figure 9 Power De-rating



Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area

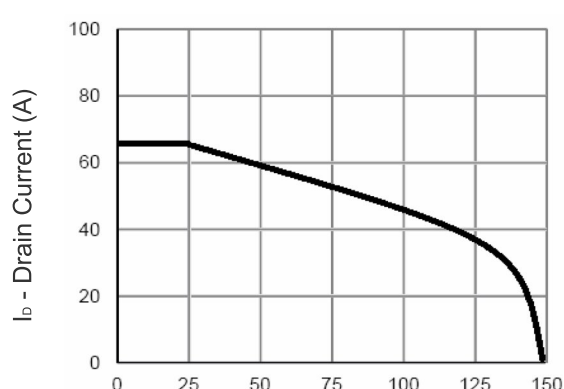

T_J -Junction Temperature(°C)

Figure 10 Current De-rating

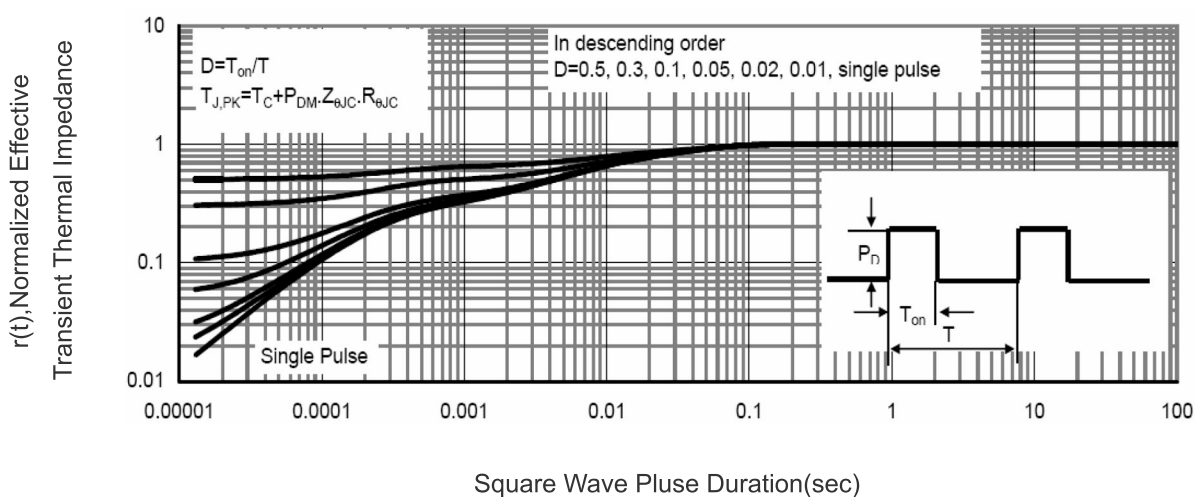
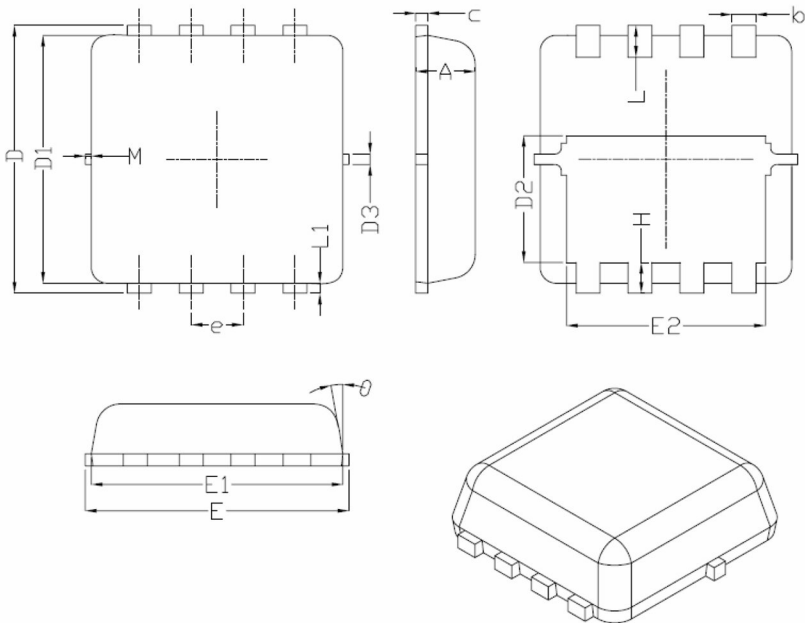


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°

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