

MJ N-Channel Enhancement Mode Power MOSFET

Description

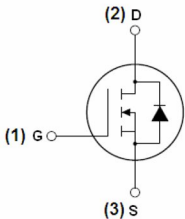
The MJ3035G uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

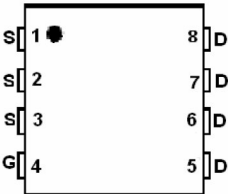
- ◆ $V_{DS}=30V, I_D=35A$
 $R_{DS(ON)}<7m\Omega$ @ $V_{GS}=10V$
 $R_{DS(ON)}<12m\Omega$ @ $V_{GS}=4.5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

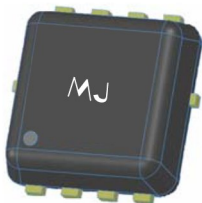
- ◆ Secondary side synchronous rectifier
- ◆ High side switch in POL DC/DC converter



Schematic diagram



Marking and pin assignment



DFN 5x6 EP top view

100% UIS TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ3035G	MJ3035G	DFN 5x6 EP	-	-	-

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	35	A
Pulsed Drain Current	I_{DM}	120	A
Maximum Power Dissipation	P_D	40	W
Derating factor		0.32	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	150	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.1	°C/W
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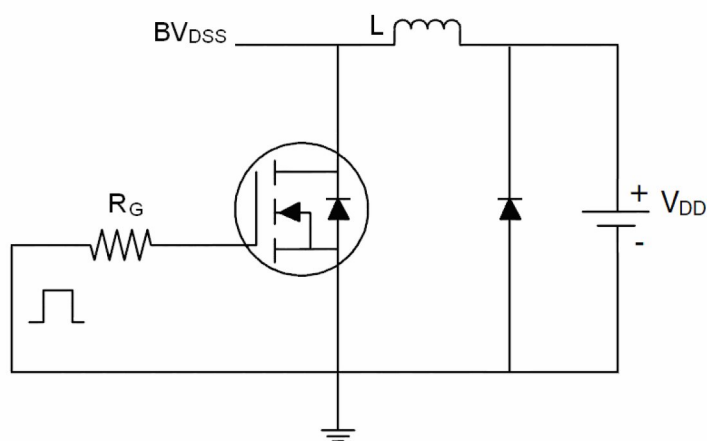
Electrical Characteristics (Tc =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1	1.6	3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =12A	-	5.9	7.0	mΩ
		V _{GS} =4.5V, I _D =10A	-	8.9	12.0	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V,I _D =12A	30	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =15V,V _{GS} =0V, F=1.0MHz	-	2330	-	PF
Output Capacitance	C _{oss}		-	460	-	PF
Reverse Transfer Capacitance	C _{rss}		-	230	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V,I _D =12A V _{GS} =10V,R _{GEN} =6Ω	-	18	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}		-	34	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =15V,I _D =12A, V _{GS} =10V	-	45	-	nC
Gate-Source Charge	Q _{gs}		-	13	-	nC
Gate-Drain Charge	Q _{gd}		-	10	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =12A	-	0.85	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	35	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =12A di/dt=100A/μs ^(Note 3)	-	-	47	nS
Reverse Recovery Charge	Q _{rr}		-	-	25	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

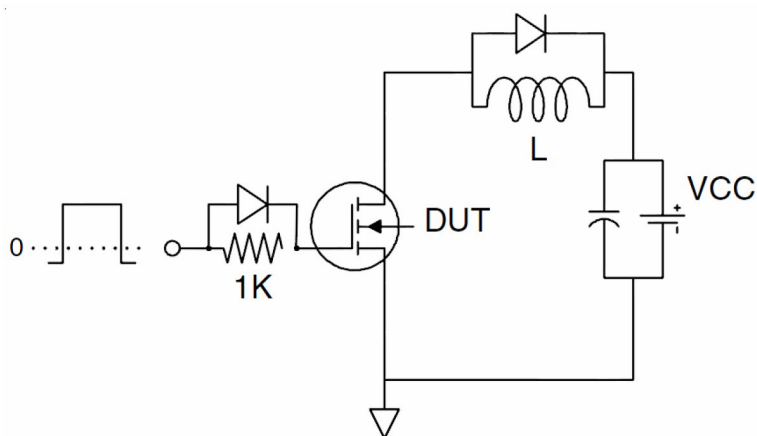
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t≤10sec.
- ③ Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition：Tj=25℃,V_{DD}=15V,V_G=10V,L=0.1mH,R_g=25Ω

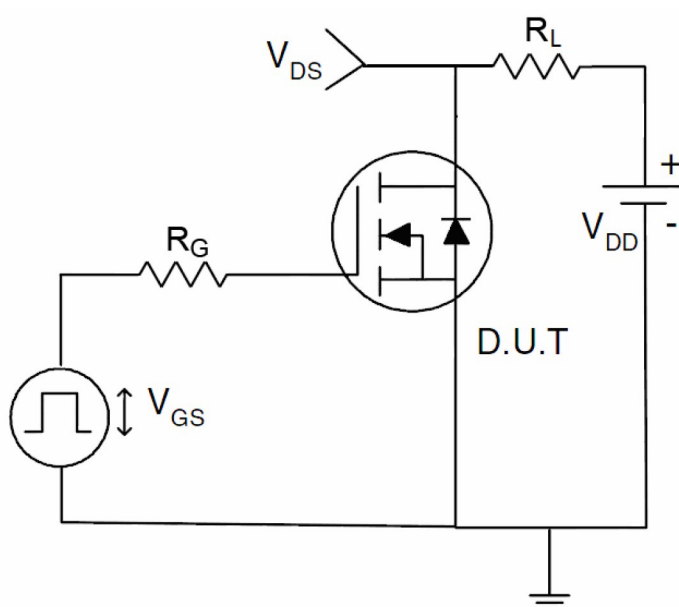
Test circuit



EAS test Circuit

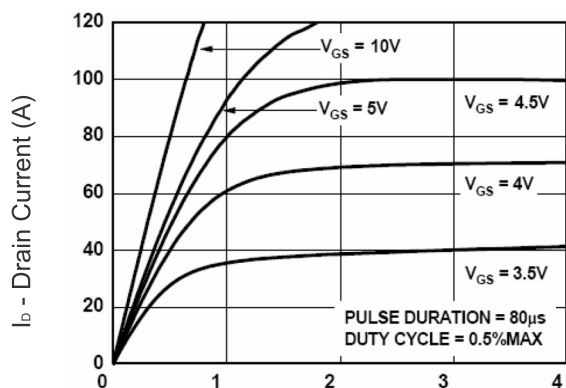


Gate charge test Circuit



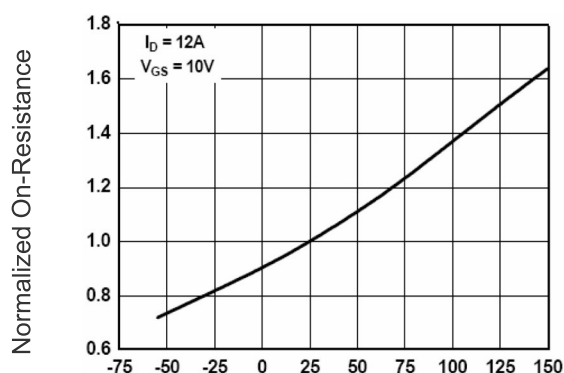
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



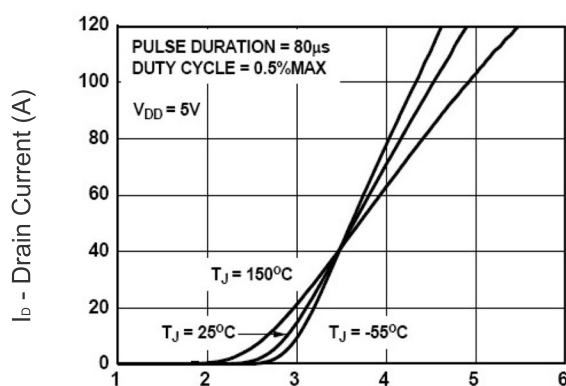
V_{DS} Drain-Source Voltage (V)

Figure 1 Output Characteristics



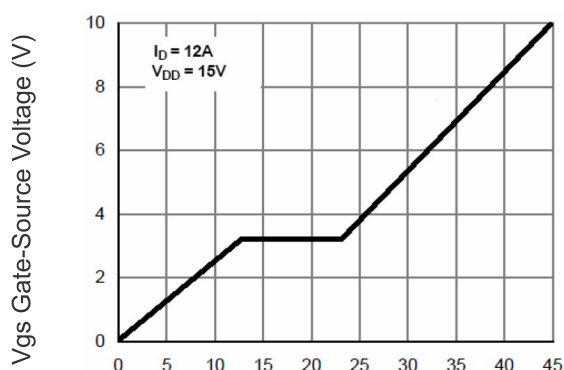
T_J -Junction Temperature($^{\circ}C$)

Figure 4 $R_{DS(on)}$ -Junction Temperature



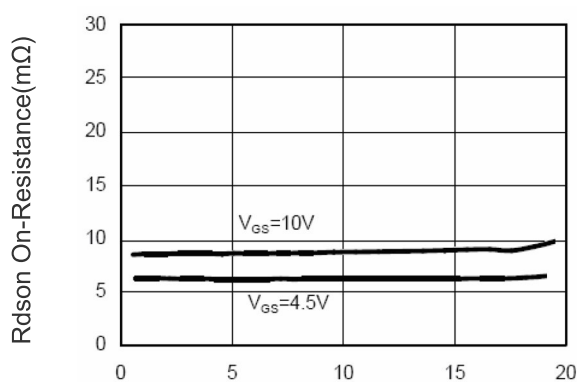
V_{GS} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



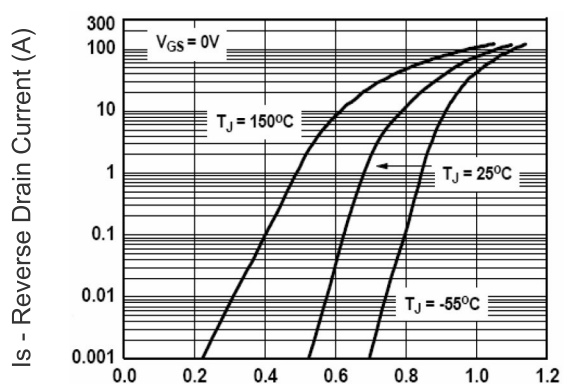
Q_g Gate Charge (nC)

Figure 5 Gate Charge



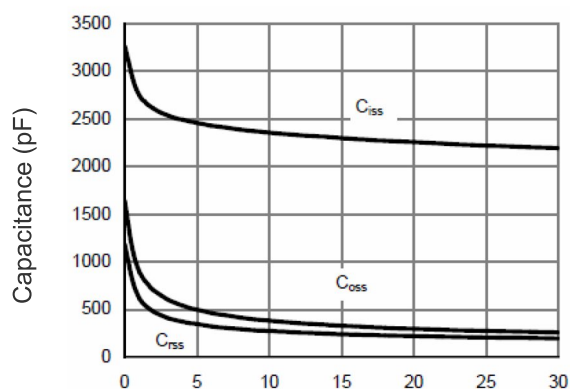
I_D - Drain Current (A)

Figure 3 $R_{DS(on)}$ - Drain Current



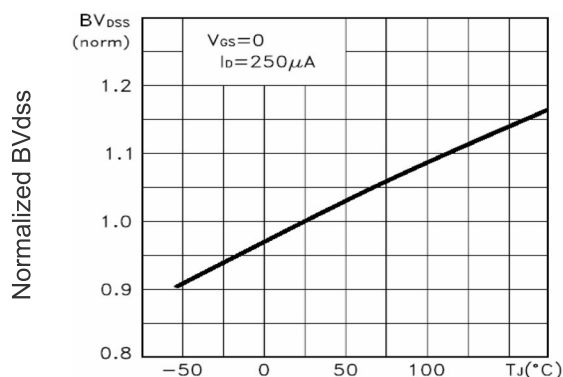
V_{SD} Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



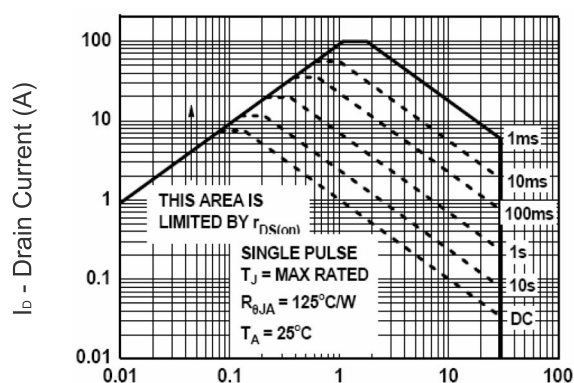
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



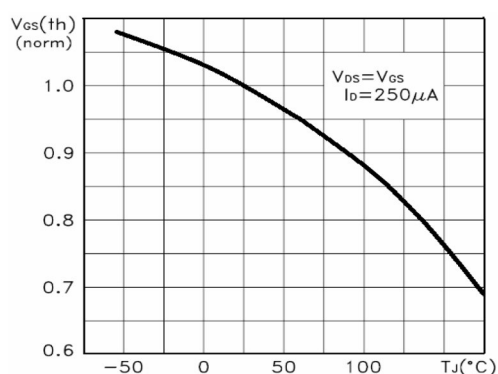
TJ -Junction Temperature(°C)

Figure 9 BVdss vs Junction Temperature



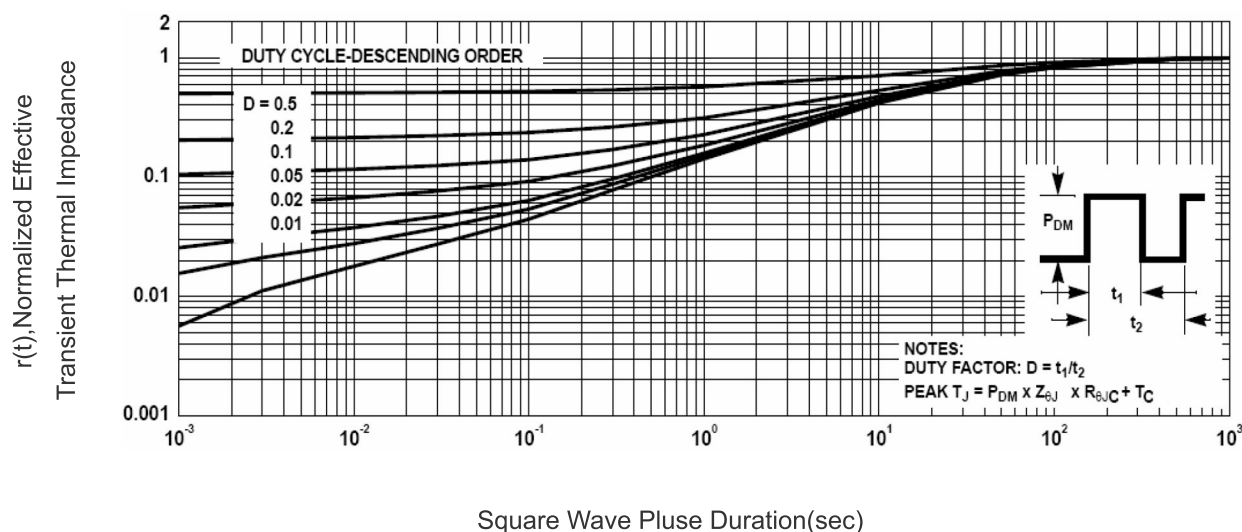
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ -Junction Temperature(°C)

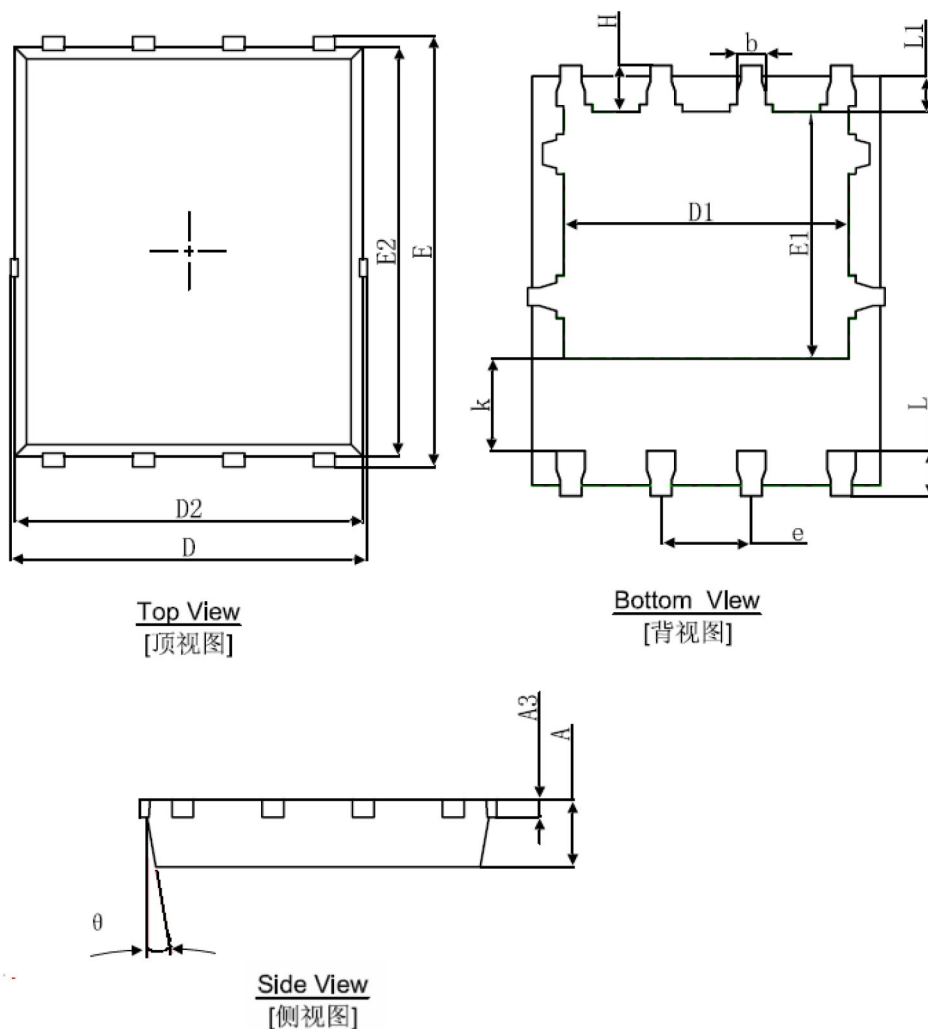
Figure 10 VGS(th) vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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