

MJ N-Channel Enhancement Mode Power MOSFET

Description

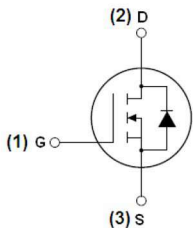
The MJ3015S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

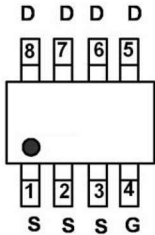
- ◆ $V_{DS} = 30V, I_D = 15A$
 $R_{DS(ON)} < 7.0m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 9.5m\Omega @ V_{GS} = 5V$
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation

Application

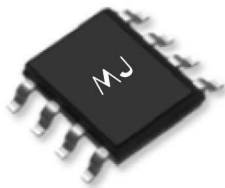
- ◆ Power switching application
- ◆ Hard Switched and High Frequency Circuits
- ◆ Uninterruptible Power Supply



Schematic diagram



Marking and pin assignment



SOP-8 top view

100% UIS TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ3015S	MJ3015S	SOP-8	-	-	-

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	15	A
Drain Current-Continuous($T_C = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	10.6	A
Pulsed Drain Current ^(Note 1)	I_{DM}	60	A
Maximum Power Dissipation	P_D	3.5	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	120	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	36	$^{\circ}C/W$
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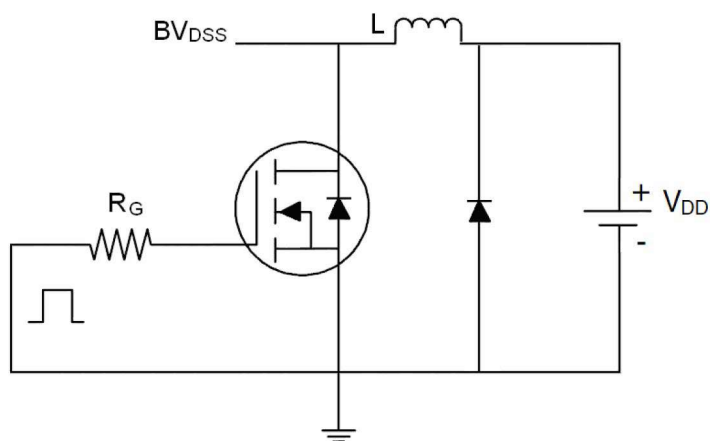
Electrical Characteristics (Tc=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V,I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1	1.4	2.4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	5.1	7.0	mΩ
		V _{GS} =4.5V, I _D =10A	-	7.3	9.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =10A	20	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =15V,V _{GS} =0V F=1.0MHz	-	1400	-	PF
Output Capacitance	C _{oss}		-	205	-	PF
Reverse Transfer Capacitance	C _{rss}		-	177	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =5V,I _D =10A V _{GS} =10V,R _{GEN} =6Ω	-	9	-	nS
Turn-on Rise Time	t _r		-	8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	28	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =15V,I _D =10A V _{GS} =10V	-	32.3	-	nC
Gate-Source Charge	Q _{gs}		-	4.9	-	nC
Gate-Drain Charge	Q _{gd}		-	6.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =10A	-	0.85	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	15	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =10A di/dt= 100A/μs <small>(Note 3)</small>	-	-	27	nS
Reverse Recovery Charge	Q _{rr}		-	-	20	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

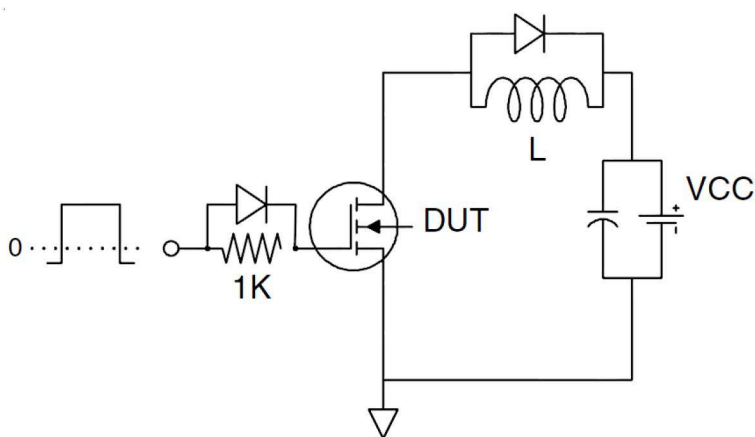
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition：T_J=25℃,V_{DD}=15V,V_G=10V,L=0.5mH,R_g=25Ω

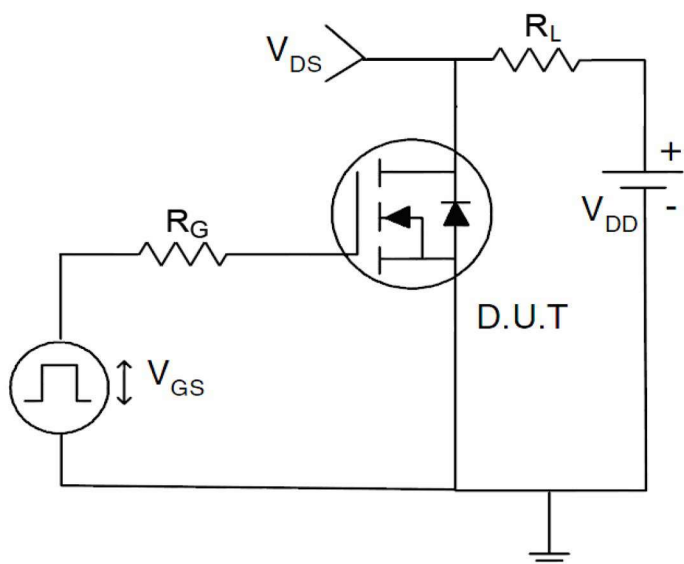
Test circuit



EAS test Circuit

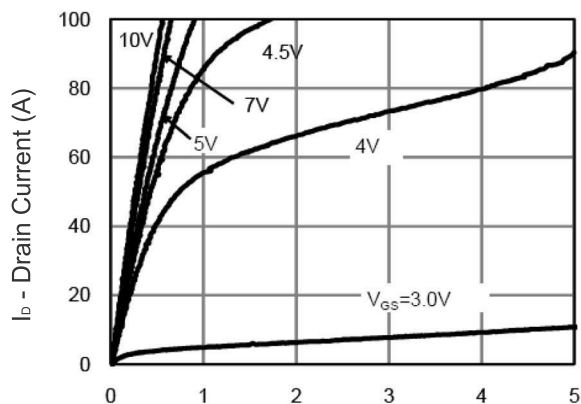


Gate charge test Circuit



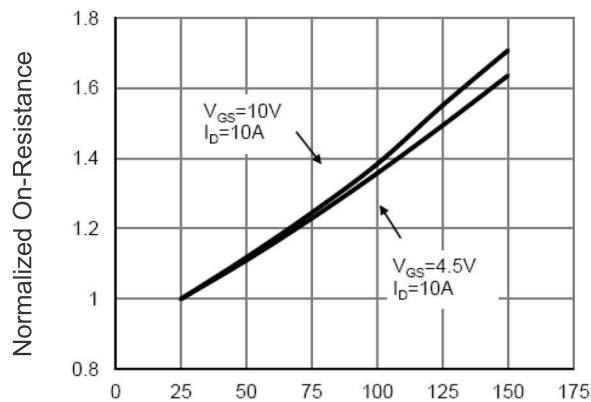
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



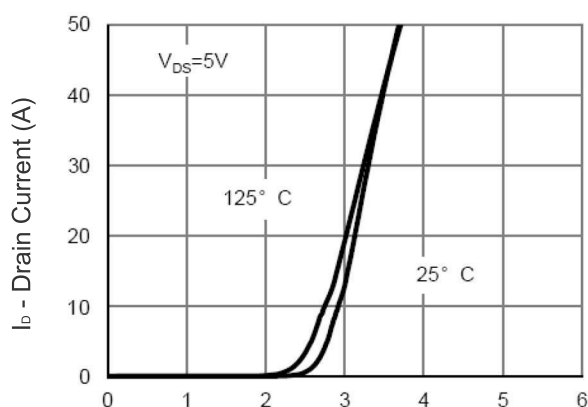
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



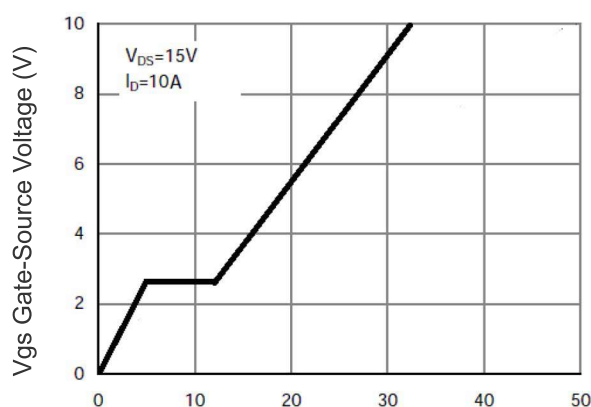
Tj -Junction Temperature(°C)

Figure 4 Rdson-Junction Temperature



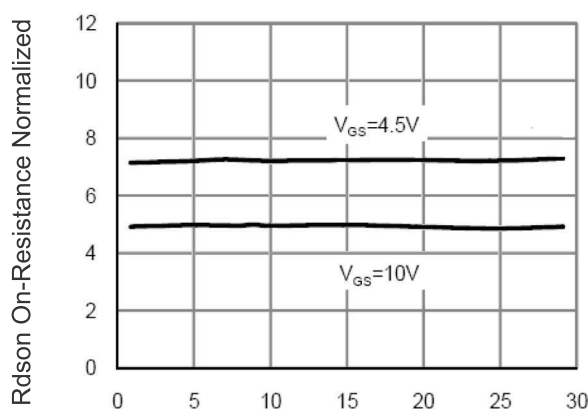
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



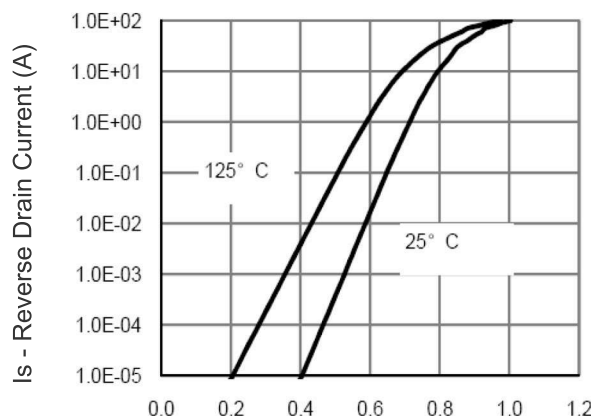
Qg Gate Charge (nC)

Figure 5 Gate Charge



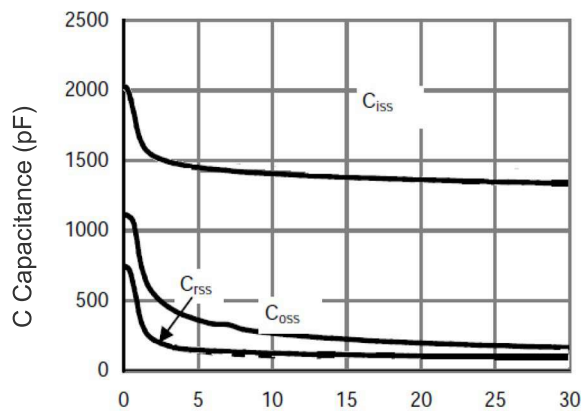
Id - Drain Current (A)

Figure 3 Rdson- Drain Current



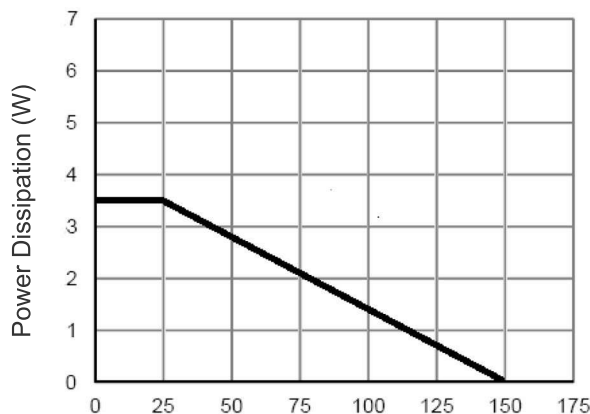
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



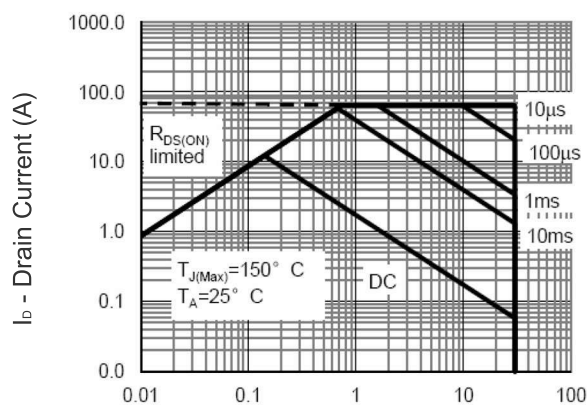
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



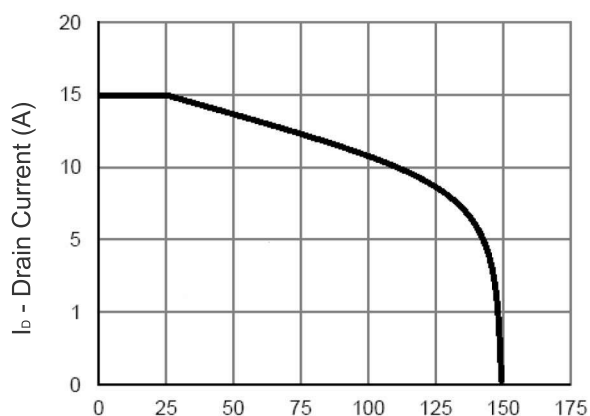
Tc-Case Temperature(°C)

Figure 9 Power De-rating



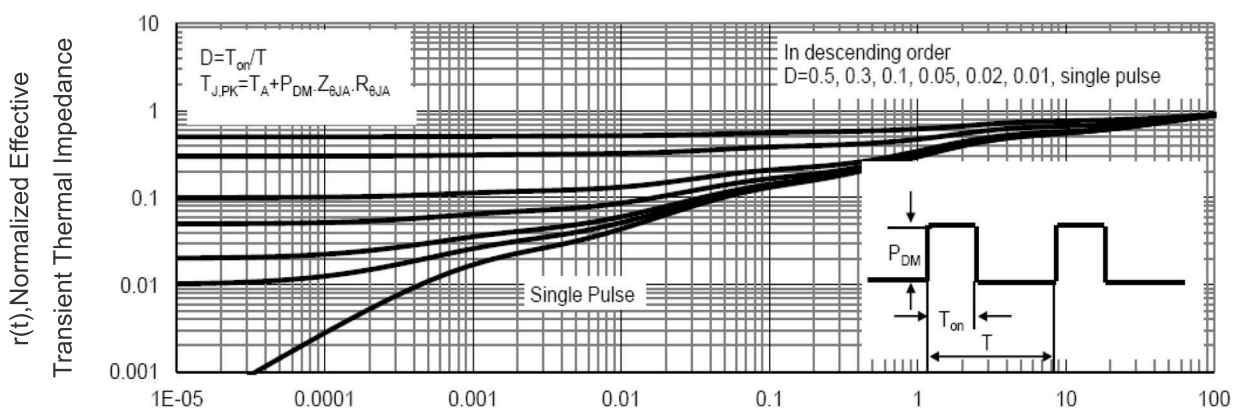
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)

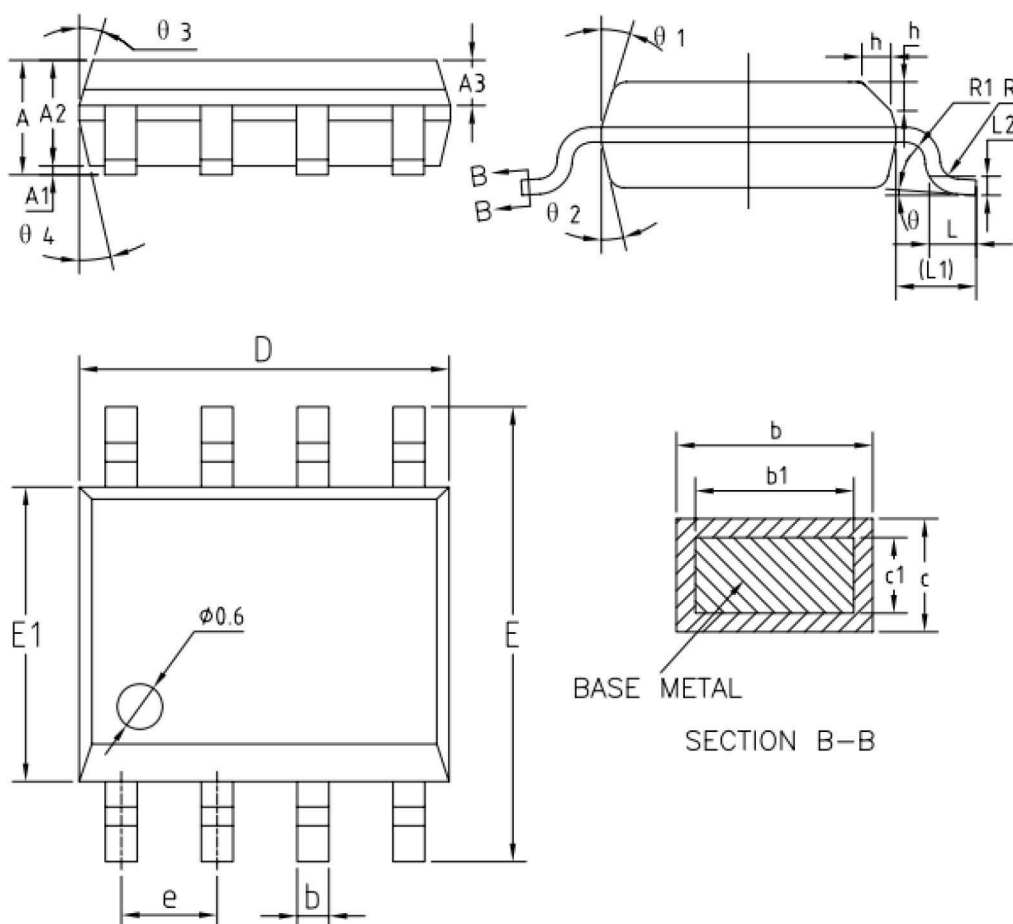
Figure10 Id Current- Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	—	0.51
b1	0.37	0.42	0.47
c	0.18	—	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	—	—
R1	0.07	—	—
h	0.30	0.40	0.50
θ	0°	—	8°
$\theta 1$	15°	17°	19°
$\theta 2$	11°	13°	15°
$\theta 3$	15°	17°	19°
$\theta 4$	11°	13°	15°

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