MJ P-Channel Enhancement Mode Power MOSFET

Description

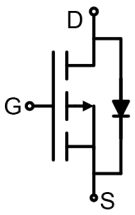
The MJ2321 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

General Features

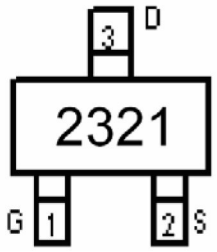
- ◆ V_{DS}=-20V,I_D=-3.9A
  $R_{DS(ON)}$<70mΩ @ V_{GS}=-2.5V
  $R_{DS(ON)}$<50mΩ @ V_{GS}=-4.5V
- ◆ High power and current handing capability
- ◆ Lead free product is acquired
- ◆ Surface Mount Package

Application

- ◆ PA switch
- ◆ Load switch
- ◆ Power management



Schematic diagram



Marking and pin Assignment

SOT-23 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
2321	MJ2321	SOT-23	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current -Continuous	I_D	-3.9	V
Drain Current-Pulsed (Note 1)	I_{DM}	-12	A
Maximum Power Dissipation	P_D	1.4	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	89	℃/W

Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=-250μA	-0.45	-0.7	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-3.3A	-	37	50	mΩ
		V_{GS}=-2.5V, I_D=-3.0A	-	48	70	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-3.0A	5	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=-10V,V_{GS}=0V, F=1.0MHz	-	560	-	PF
Output Capacitance	C_{oss}		-	80	-	PF
Reverse Transfer Capacitance	C_{rss}		-	70	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-10V,I_D=-3.3A , R_L=2.2Ω,V_{GS}=-4.5V, Rg=6Ω	-	12	-	nS
Turn-on Rise Time	t_r		-	35	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	40	-	nS
Total Gate Charge	Q_g	V_{DS}=-10V,I_D=-3.3A, V_{GS} =-4.5V	-	8.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.2	-	nC
Gate-Drain Charge	Q_{gd}		-	2.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-3.9A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-3.9	A

Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

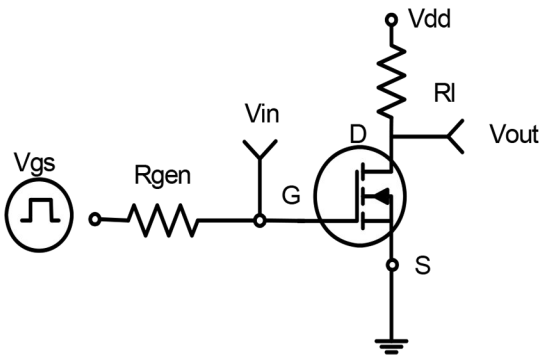


Figure 1 Switching Test Circuit

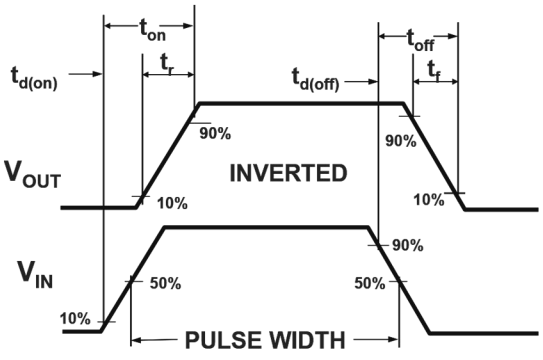


Figure 2 Switching Waveforms

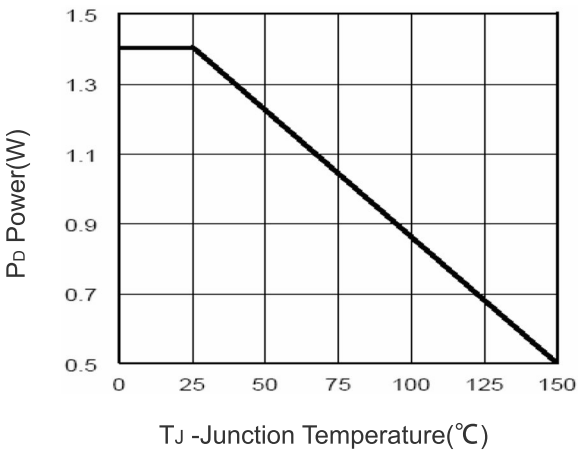


Figure 3 Power Dissipation

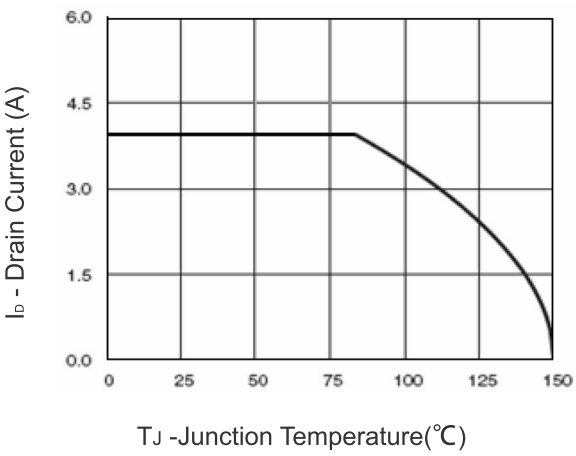


Figure 4 Drain Current

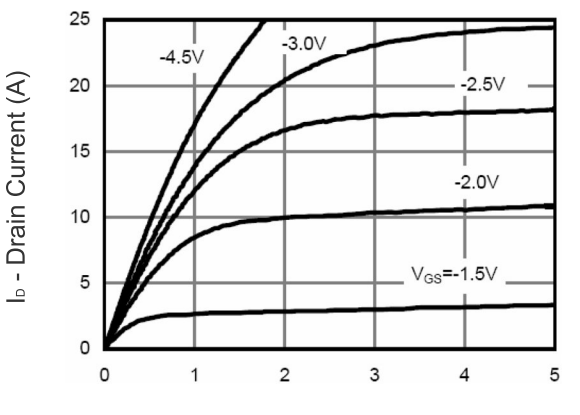


Figure 5 Output Characteristics

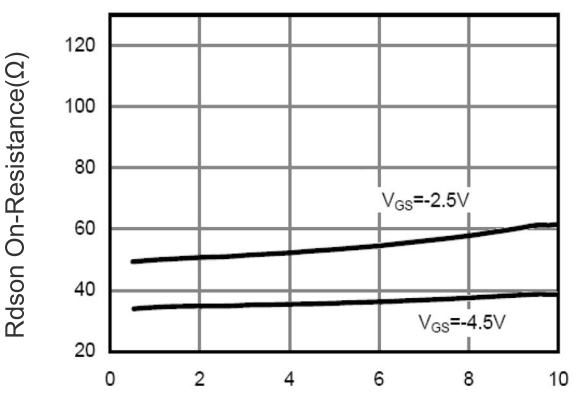


Figure 6 Drain-Source On-Resistance

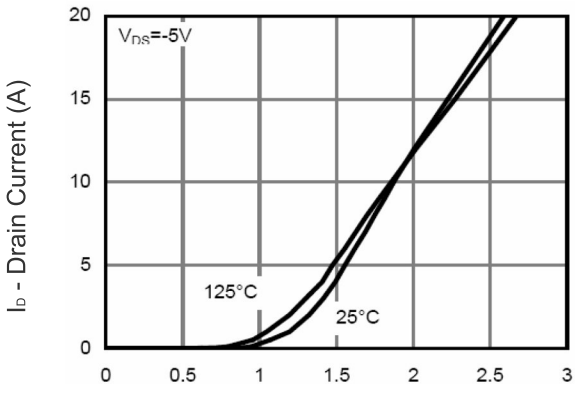


Figure 7 Transfer Characteristics

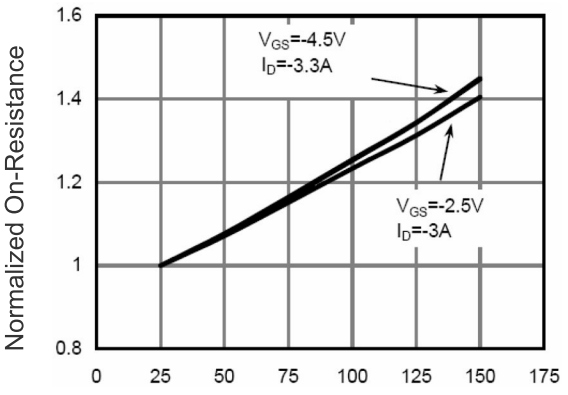


Figure 8 Drain-Source On-Resistance

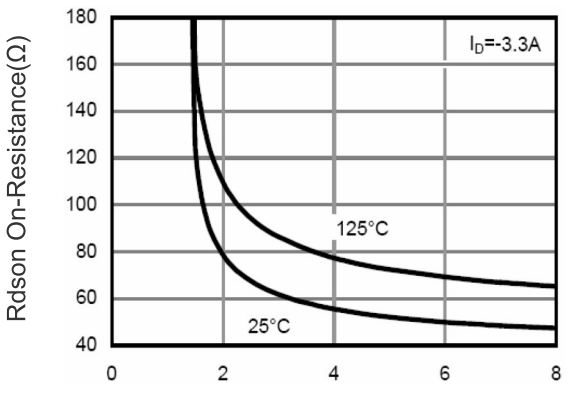


Figure 9 Rdson vs Vgs

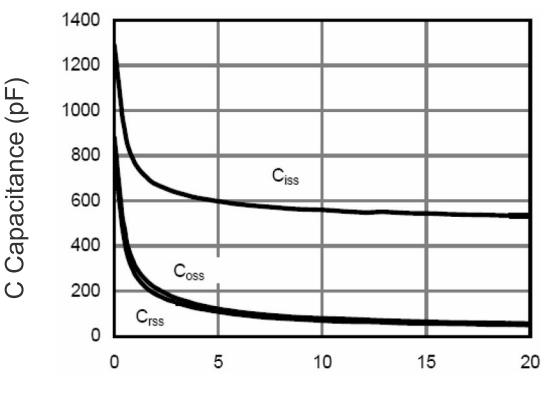


Figure 10 Capacitance vs Vds

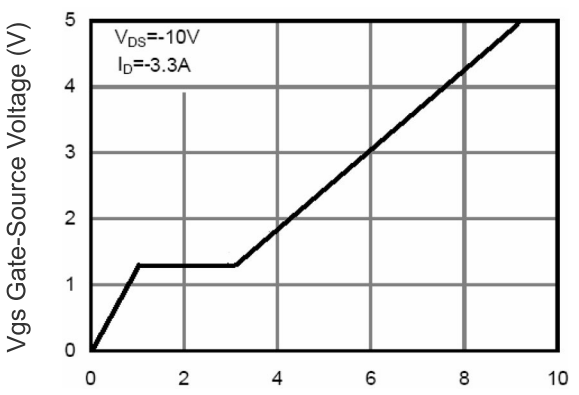


Figure 11 Gate Charge

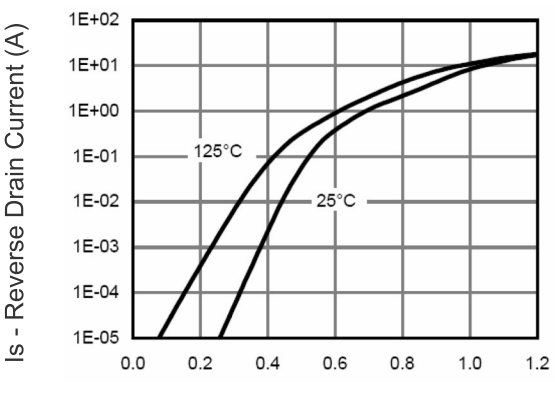
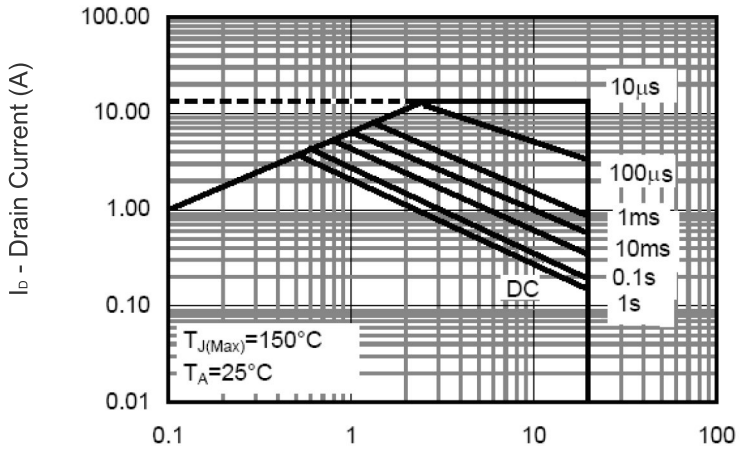
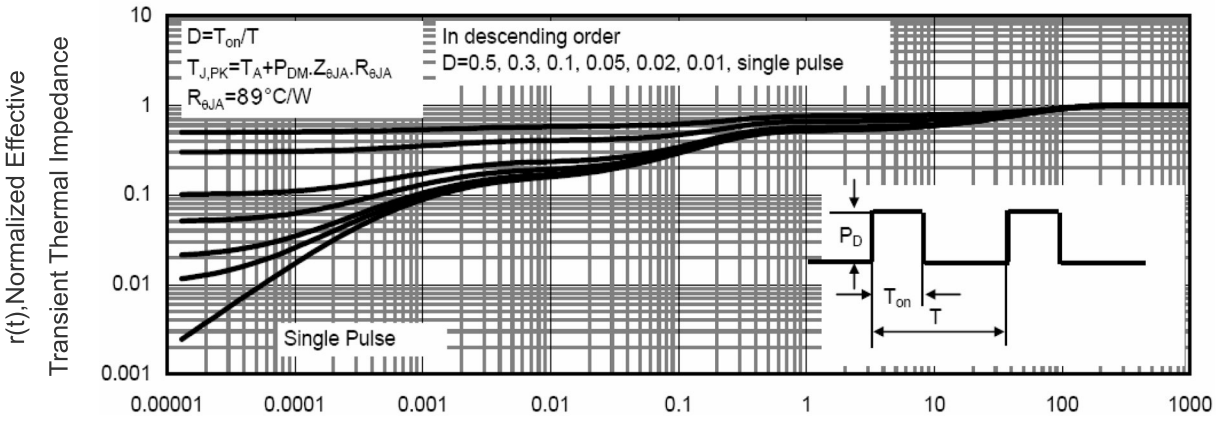


Figure 12 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)

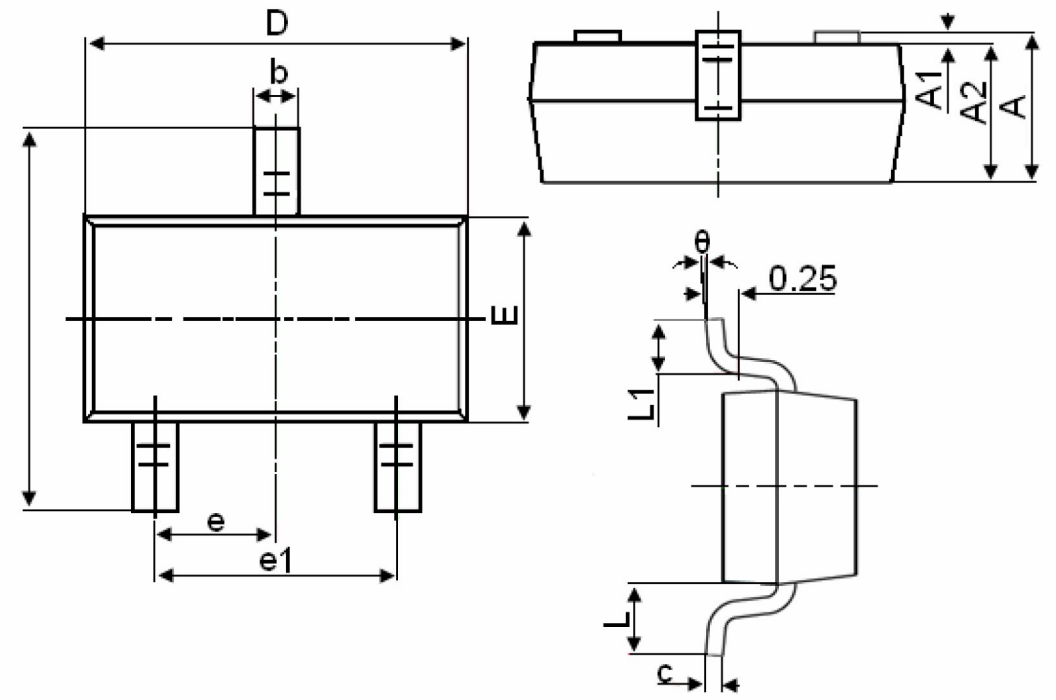
Figure 13 Safe Operation Area



Square Wave Pluse Duration(sec)

Figure 14 Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

Notes:

① All dimensions are in millimeters.
② Tolerance ±0.10mm (4 mil) unless otherwise specified
③ Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
④ Dimension L is measured in gauge plane.
⑤ Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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