

MJ P-Channel Enhancement Mode Power MOSFET

Description

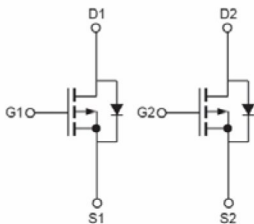
The MJ20PD05 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

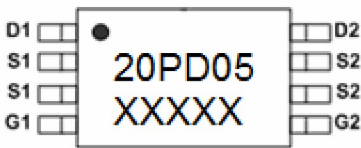
- ◆ $V_{DS} = -20V, I_D = -5A$
 $R_{DS(ON)} < 30m\Omega @ V_{GS} = 2.5V$
 $R_{DS(ON)} < 22m\Omega @ V_{GS} = 4.5V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface Mount Package

Application

- ◆ Battery protection
- ◆ Load switch
- ◆ Power management



Schematic diagram



Marking and pin Assignment



TSSOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
20PD05	MJ20PD05	TSSOP-8	Ø330mm	12mm	3000 units

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-5	A
Pulsed Drain Current ^(Note 1)	I_{DM}	-20	A
Maximum Power Dissipation	P_D	-1.6	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	78	°C/W
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Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-20	-21	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±12V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-0.5	-0.7	-1.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-5A	-	24.8	30	mΩ
		V _{GS} =-2.5V, I _D =-5A	-	32.5	40	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V,I _D =-5A	-	15	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =-10V,V _{GS} =0V, F=1.0MHz	-	1025	-	PF
Output Capacitance	C _{oss}		-	167	-	PF
Reverse Transfer Capacitance	C _{rss}		-	119	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-10V, ,I _D =-5A V _{GS} =-4.5V,R _{GEN} =6Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	15	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	40	-	nS
Total Gate Charge	Q _g	V _{DS} =-10V,I _D =-5A, V _{GS} =-4.5V	-	13	-	nC
Gate-Source Charge	Q _{gs}		-	2	-	nC
Gate-Drain Charge	Q _{gd}		-	3.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =-5A	-	-0.75	-1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	-5	A

Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

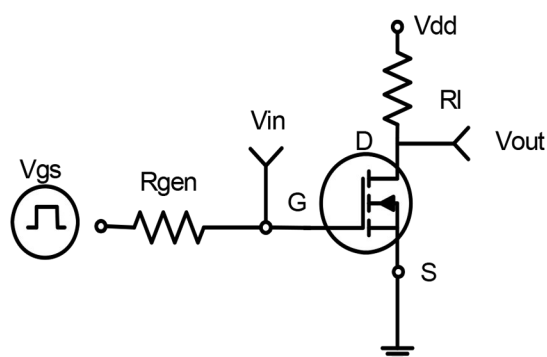


Figure 1 Switching Test Circuit

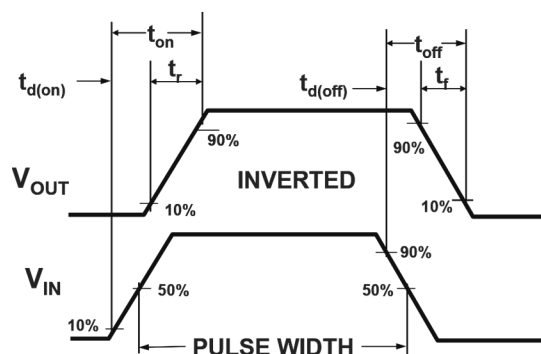


Figure 2 Switching Waveforms

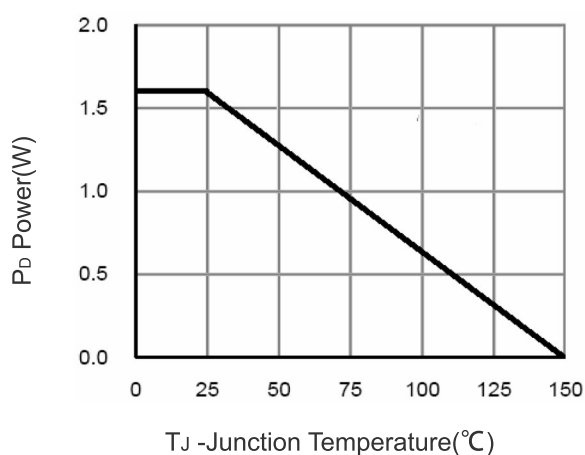


Figure 3 Power Dissipation

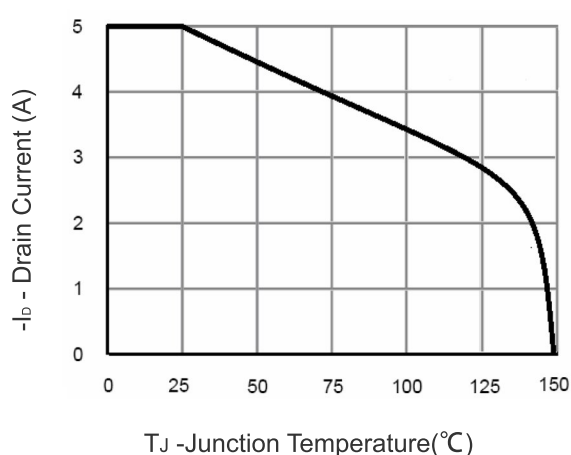


Figure 4 Drain Current

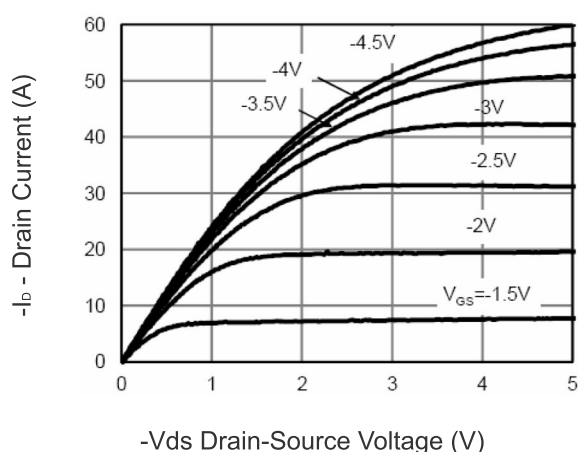


Figure 5 Output Characteristics

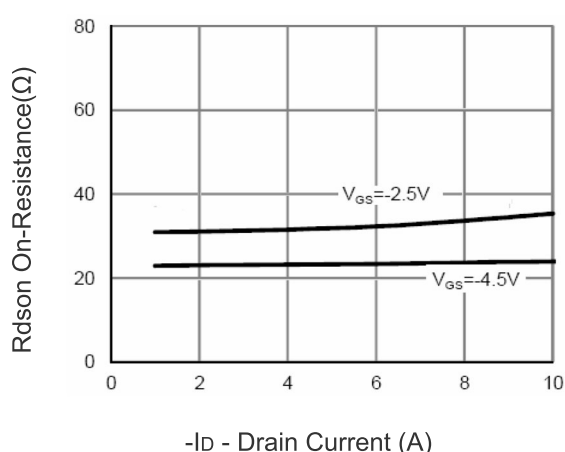


Figure 6 Drain-Source On-Resistance

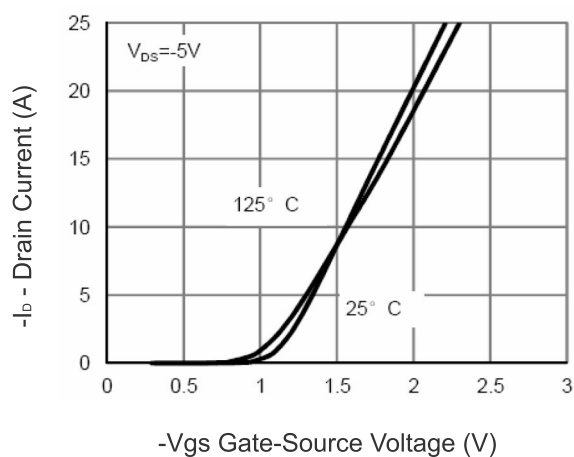


Figure 7 Transfer Characteristics

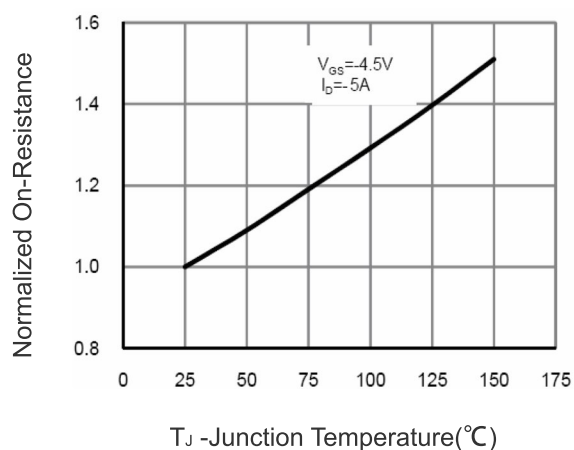


Figure 8 Drain-Source On-Resistance

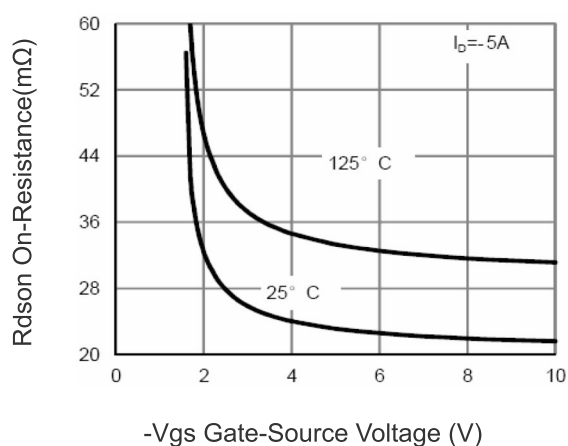


Figure 9 Rdson vs Vgs

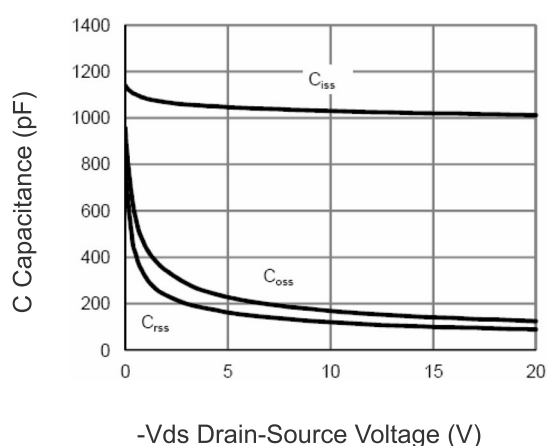


Figure 10 Capacitance vs Vds

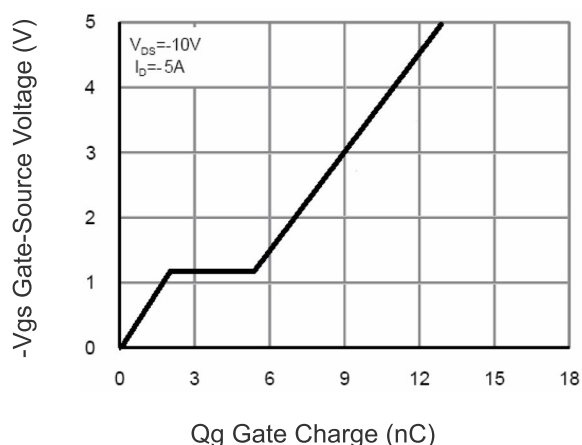


Figure 11 Gate Charge

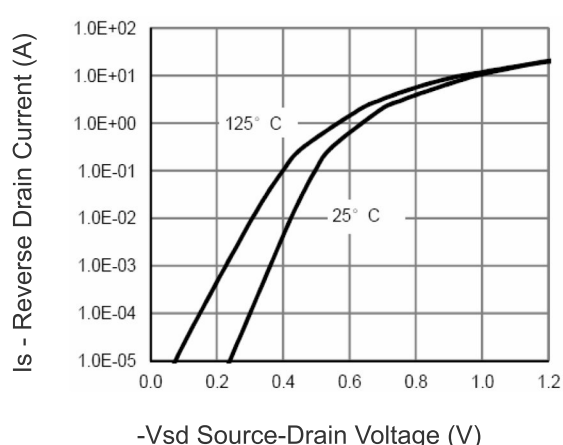


Figure 12 Source- Drain Diode Forward

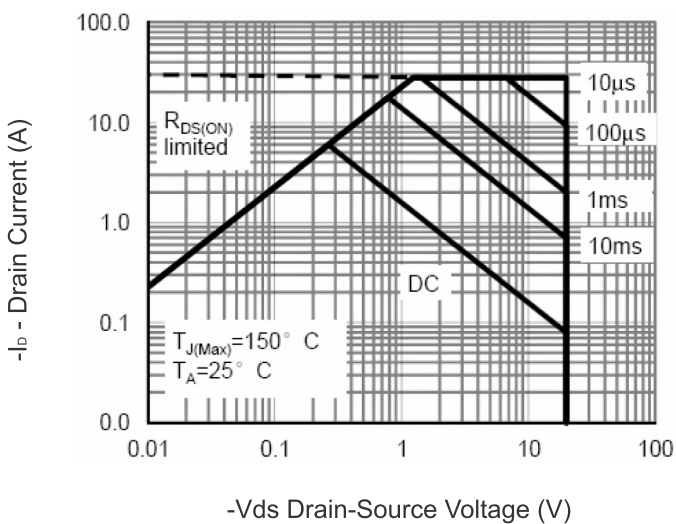


Figure 13 Safe Operation Area

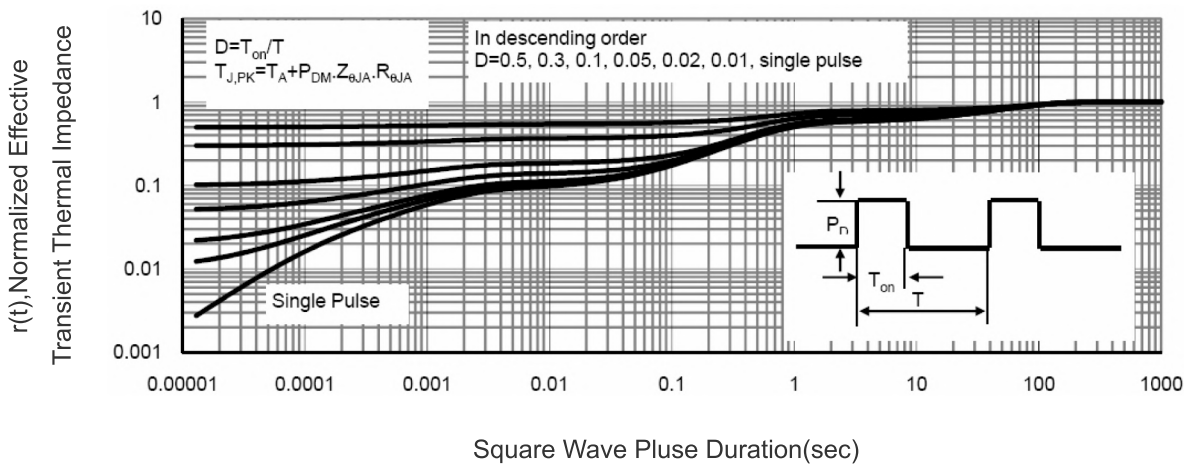
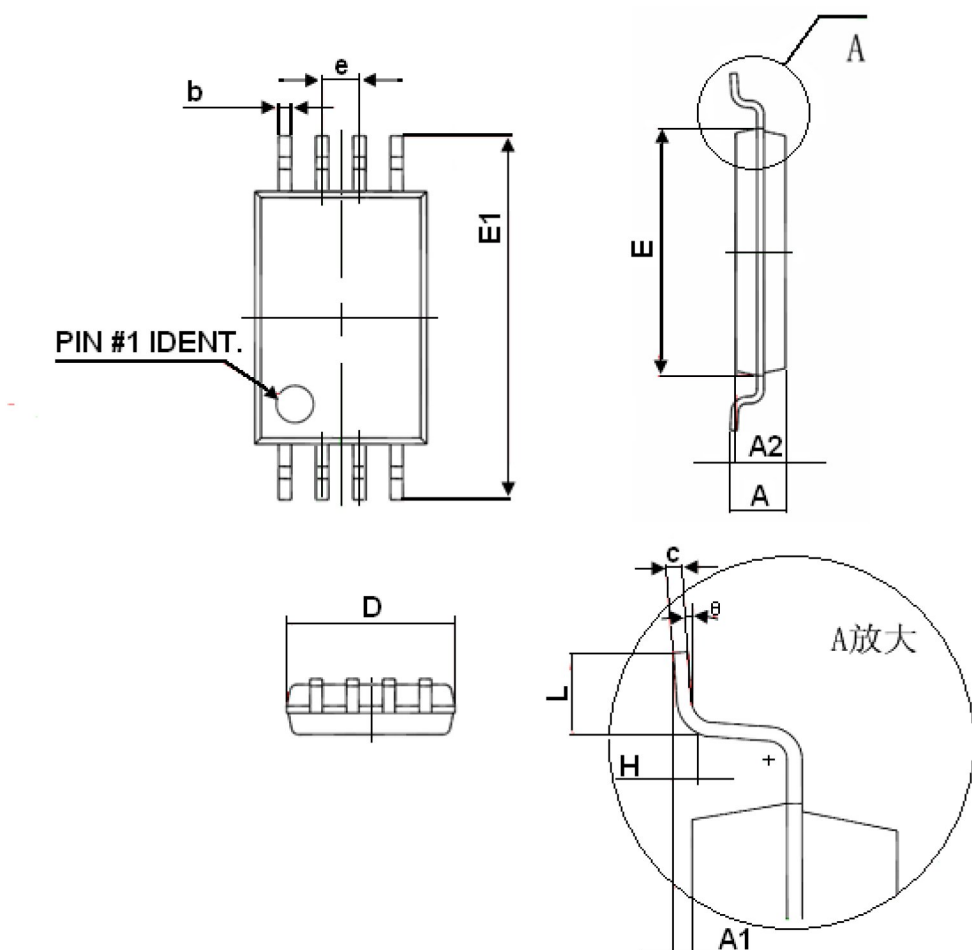


Figure 14 Normalized Maximum Transient Thermal Impedance

Tssop-8 Package Information



Symbol	Dimensions In Millimeters	
	Min	Max
D	2.900	3.100
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A		1.100
A2	0.800	1.000
A1	0.020	0.150
e	0.65(BSC)	
L	0.500	0.700
H	0.25(TYP)	
θ	1°	7°

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