



# MJ P-Channel Enhancement Mode Power MOSFET

#### Description

The MJ20P45Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

#### **General Features**

- ♦ VDS=-20V,ID=-45A

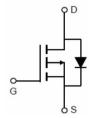
  RDS(ON)<7mΩ @ VGS=-4.5V

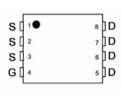
  RDS(ON)<9mΩ @ VGS=-2.5V

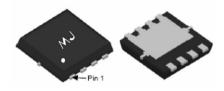
  RDS(ON)<12mΩ @ VGS=-1.8V
- ♦ High density cell design for ultra low Rdson
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high EAS
- ◆ Excellent package for good heat dissipation

#### Application

- ◆ Load switch
- Battery protection







Schematic diagram

Pin Assignment

DFN 3.3x3.3 top view

## Package Marking and Ordering Information

Device	Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ2	0P45Q	MJ20P45Q	DFN 3.3x3.3-8L	-	-	-

## Absolute Maximum Ratings (Tc =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	-20	V
Gate-Source Voltage	Vgs	±10	V
Drain Current-Continuous	ΙD	-45	А
Drain Current-Continuous(Tc =100°C)	<b>I</b> D(100℃)	-35	А
Pulsed Drain Current	Ідм	-200	А
Maximum Power Dissipation	PD	80	W
Single pulse avalanche energy (Note 5)	Eas	180	mJ
Derating factor		0.64	W/°C
Operating Junction and Storage Temperature Range	Тл ,Тѕтс	-55 To 150	°C

#### Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	RөJA	1.6	°C/W
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# Electrical Characteristics (T<sub>A</sub> =25°Cunless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BVpss	V <sub>GS</sub> =0V I <sub>D</sub> =-250µA	-20	_	-	V
Zero Gate Voltage Drain Current	Ipss	Vps=-16V,Vgs=0V	-	-	1	μA
Gate-Body Leakage Current	Igss	V <sub>DS</sub> =±10V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)	·					
Gate Threshold Voltage	VGS(th)	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =-250μA	-0.4	-0.6	-1.0	V
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A	-	5.8	7	mΩ
Drain-Source On-State Resistance	Rds(ON)	Vgs=-2.5V, Ip=-20A	-	7.2	9	mΩ
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-20A	-	9	12	mΩ
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =-5V,I <sub>D</sub> =-20A	80	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	Clss	V <sub>DS</sub> =-10V,V <sub>GS</sub> =0V, F=1.0MHz	-	3500	-	PF
Output Capacitance	Coss		-	577	-	PF
Reverse Transfer Capacitance	Crss	-	-	445	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>		-	18	-	nS
Turn-on Rise Time	tr	V <sub>DD</sub> =-10V, R <sub>GEN</sub> =3Ω	-	42	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>	V <sub>GS</sub> =-4.5V,R <sub>L</sub> =0.5Ω	-	85	-	nS
Turn-Off Fall Time	tr	-	-	23	-	nS
Total Gate Charge	Qg		-	55	-	nC
Gate-Source Charge	Qgs	V <sub>DS</sub> =-10V,I <sub>D</sub> =-20A, V <sub>GS</sub> =-4.5V	-	10	-	nC
Gate-Drain Charge	Qgd	-	-	15	-	nC
Drain-Source Diode Characteristics	'	1			ı	1
Diode Forward Voltage (Note 3)	VsD	V <sub>GS</sub> =0V,I <sub>S</sub> =-20A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	-45	А
Reverse Recovery Time	trr	TJ=25°C, IF=-10A	-	47	-	nS
Reverse Recovery Charge	Qrr	di/dt=100A/µs (Note 2)	-	53	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is n	egligible(tu	ırn-on is d	ominated b	y LS+L

#### Notes:

- ${\color{blue}\textbf{\textcircled{1}}} \ \, \text{Repetitive Rating: Pulse width limited by maximum junction temperature.}$
- ② Surface Mounted on FR4 Board,  $t \le 10$  sec.
- ③ Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4 Guaranteed by design, not subject to production
- $\bigcirc$  Eas condition: Tj=25°C,VDD=-10V,VG=-10V,L=0.5mH,Rg=25 $\Omega$



## Typical Electrical and Thermal Characteristics

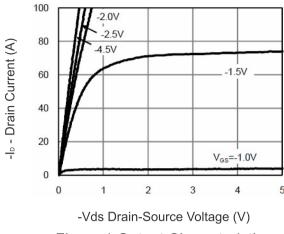
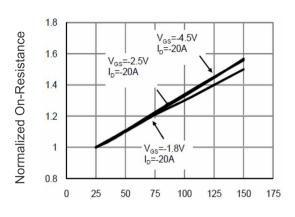


Figure 1 Output Characteristics



TJ -Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature

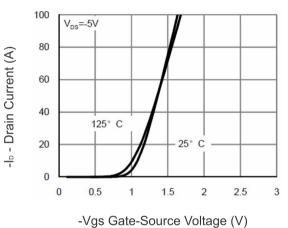
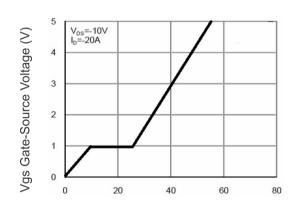


Figure 2 Transfer Characteristics



Qg Gate Charge (nC)
Figure 5 Gate Charge

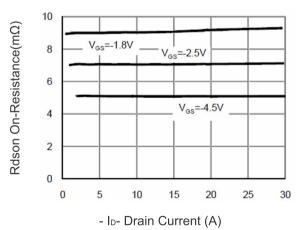
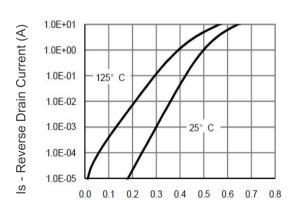


Figure 3 Rdson- Drain Current



-Vsd Source-Drain Voltage (V)
Figure 6 Drain-Source On-Resistance



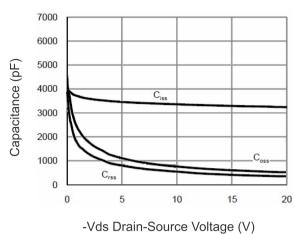
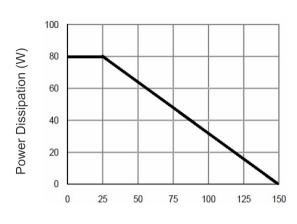


Figure 7 Capacitance vs Vds



T<sub>J</sub> -Junction Temperature(°C) Figure 9 Power De-rating

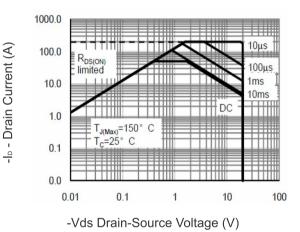
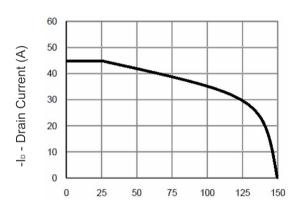
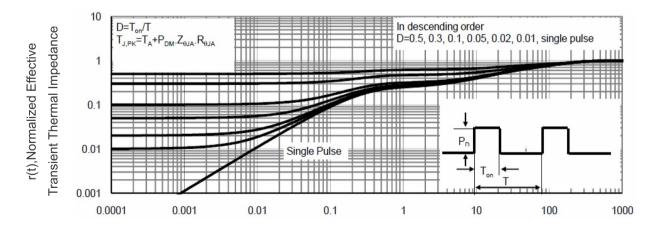


Figure 8 Safe Operation Area



T<sub>J</sub> -Junction Temperature(°C) Figure 10 -Current De-rating



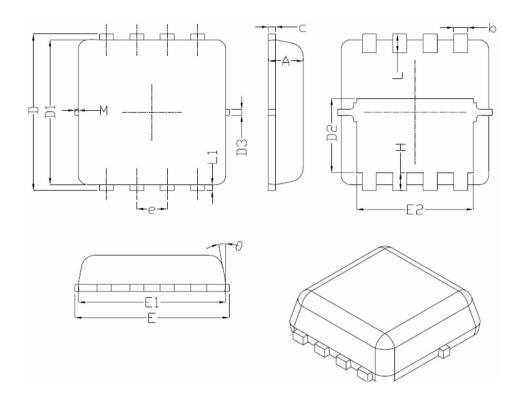
Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance





# DFN3.3X3.3 EP Package Information



CIVI (D.O.I.	DIMENSI	ONAL RE	QMTS	
SYMBOL	MIN	NOM	MAX	
A	0.70	0.75	0.80	
b	0.25	0.30	0.35	
c	0.10	0.15	0.25	
D	3.25	3.35	3.45	
D1	3.00	3.10	3.20	
D2	1.48	1.58	1.68	
D3		0.13		
E	3.20	3.30	3.40	
E1	3.00	3.15	3.20	
E2	2.39	2.49	2.59	
e	0.65BSC			
H	0.30	0.39	0.50	
L	0.30	0.40	0.50	
L1		0.13		
$\theta$		10°	12°	
M	*	*	0.15	
* Not specified				





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