

MJ N-Channel Enhancement Mode Power MOSFET

Description

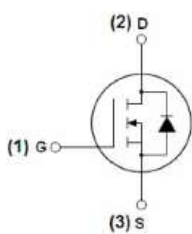
The MJ2030K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

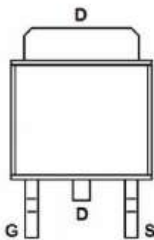
- ◆ $V_{DS} = 20V, I_D = 30A$
 $R_{DS(ON)} < 12m\Omega$ @ $V_{GS} = 10V$ (Typ: 10.5m Ω)
 $R_{DS(ON)} < 13m\Omega$ @ $V_{GS} = 4.5V$ (Typ: 11m Ω)
 $R_{DS(ON)} < 18m\Omega$ @ $V_{GS} = 2.5V$ (Typ: 14m Ω)
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

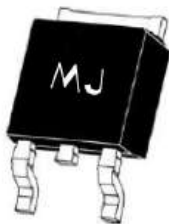
- ◆ Power switching application
- ◆ Load switching
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252-2L top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ2030K	MJ2030K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_A =25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous(T _C =100°C)	$I_{D(100^{\circ}C)}$	21	A
Pulsed Drain Current	I_{DM}	100	A
Maximum Power Dissipation	P_D	40	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	150	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.8	°C/W
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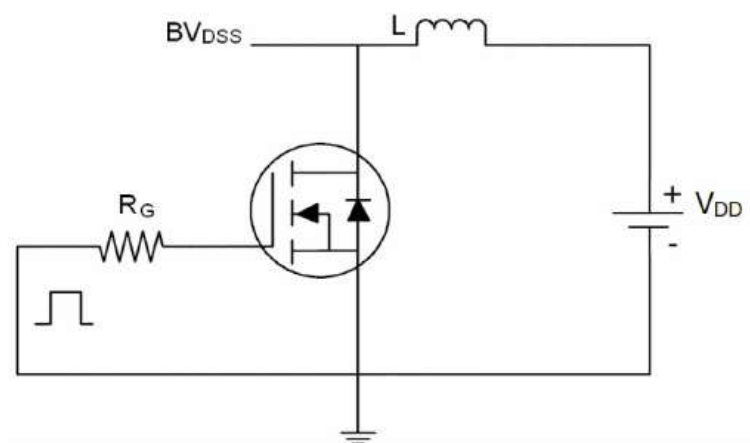
Electrical Characteristics (T_A =25°Cunless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±12V,V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	0.5	0.7	1.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	10.5	12	mΩ
		V _{GS} =4.5V, I _D =20A	-	11	13	mΩ
		V _{GS} =2.5V, I _D =20A	-	14	18	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =20A	10	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =10V,V _{GS} =0V F=1.0MHz	-	1544	-	PF
Output Capacitance	C _{oss}		-	210.1	-	PF
Reverse Transfer Capacitance	C _{rss}		-	201.4	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{GS} =10V,V _{DS} =10V R _L =0.5Ω,R _{GEN} =3Ω	-	4.5	-	nS
Turn-on Rise Time	t _r		-	9.2	-	nS
Turn-Off Delay Time	t _{d(off)}		-	18.7	-	nS
Turn-Off Fall Time	t _f		-	3.3	-	nS
Total Gate Charge	Q _g	V _{GS} =4.5V,V _{DS} =10V I _D =20A	-	23.5	-	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	nC
Gate-Drain Charge	Q _{gd}		-	5.75	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	30	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =20A di/dt=100A/μs <small>(Note 3)</small>	-	18	-	nS
Reverse Recovery Charge	Q _{rr}		-	9.5	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

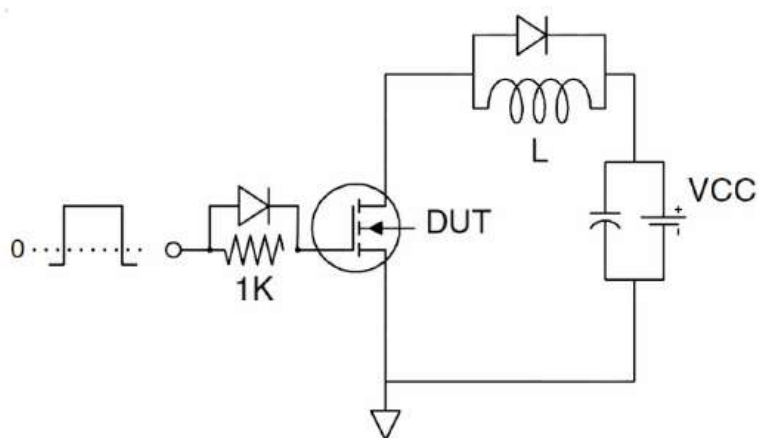
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C,V_{DD}=10V,V_G=10V,L=0.5mH,R_g=25Ω

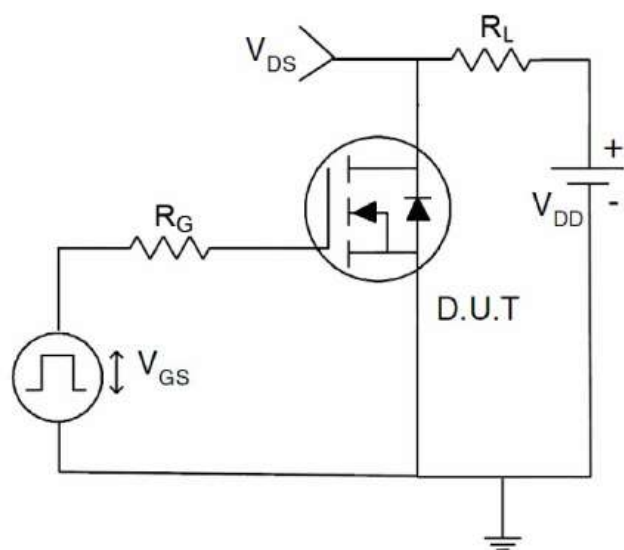
Test circuit



EAS test Circuit

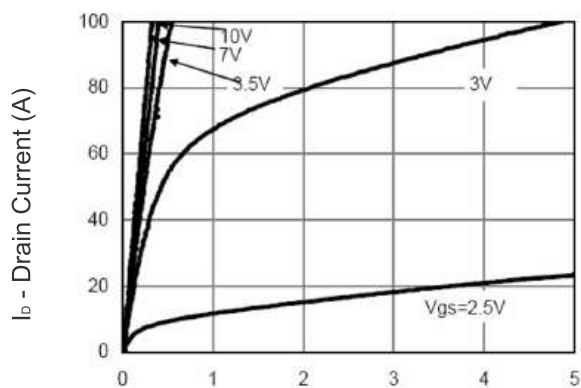


Gate charge test Circuit



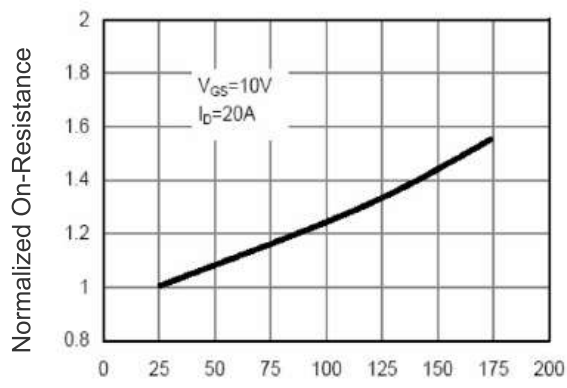
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



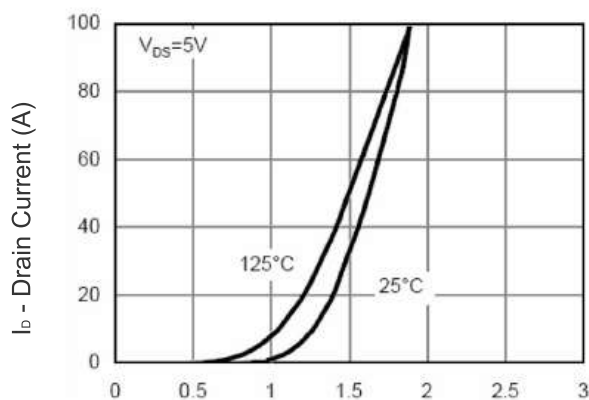
V_{DS} Drain-Source Voltage (V)

Figure 1 Output Characteristics



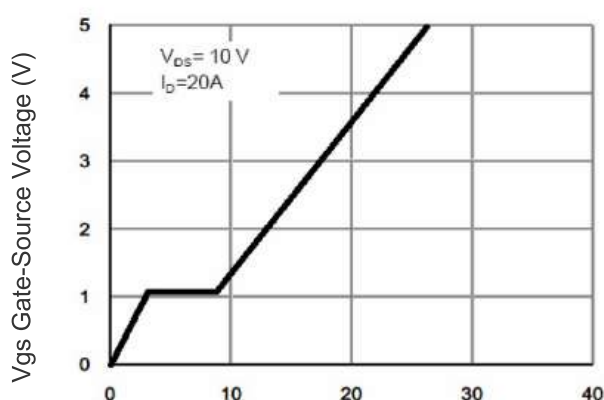
T_J -Junction Temperature($^{\circ}C$)

Figure 4 $R_{DS(on)}$ -Junction Temperature



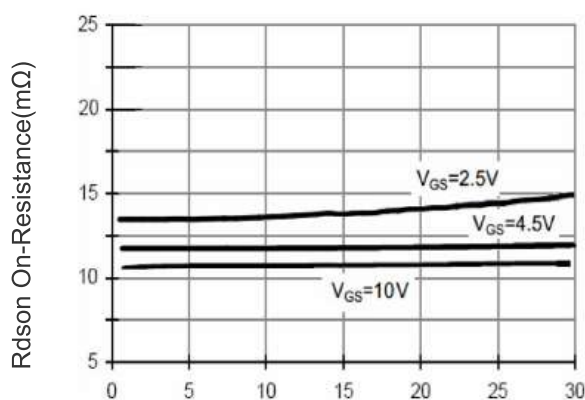
V_{GS} Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



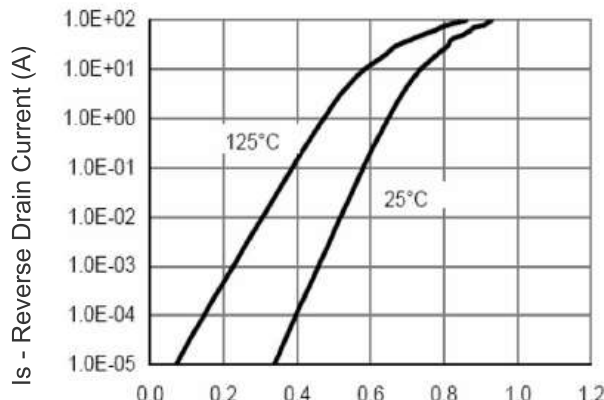
Q_g Gate Charge (nC)

Figure 5 Gate Charge



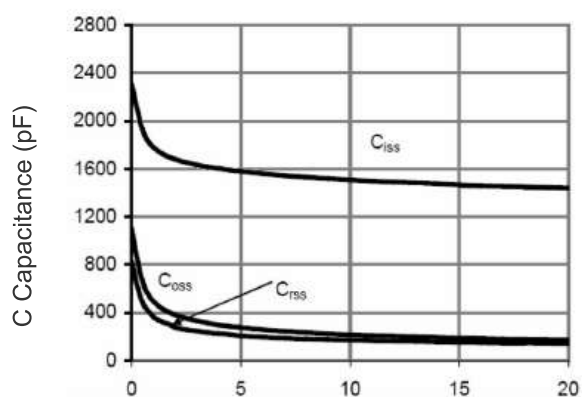
I_D - Drain Current (A)

Figure 3 $R_{DS(on)}$ - Drain Current

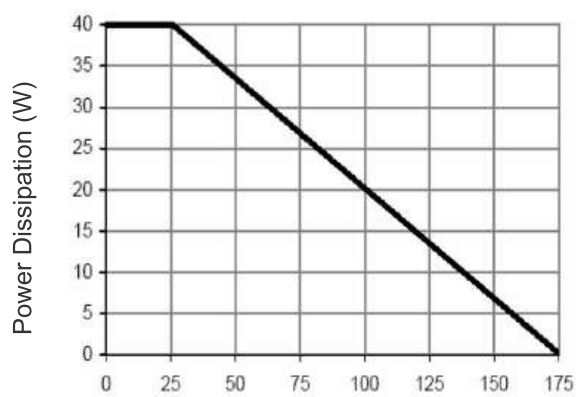


V_{SD} Source-Drain Voltage (V)

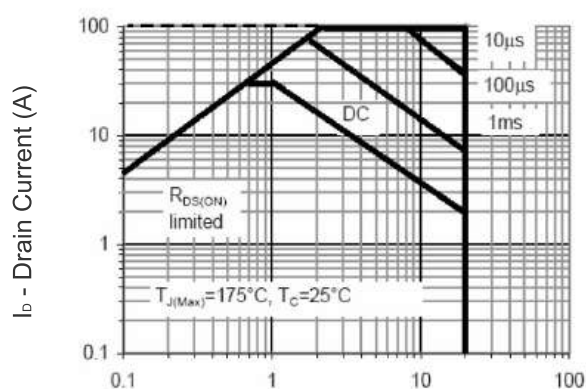
Figure 6 Source- Drain Diode Forward



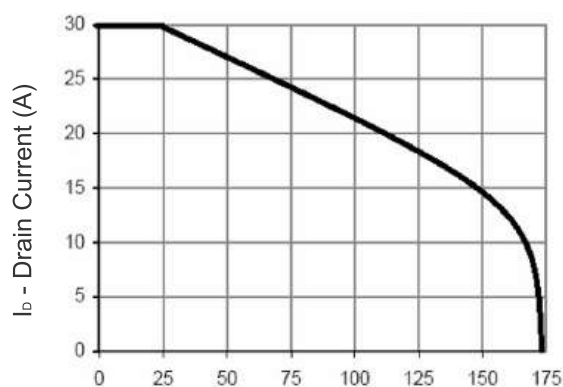
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



TJ -Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



TJ -Junction Temperature(°C)
Figure 10 Current De-rating

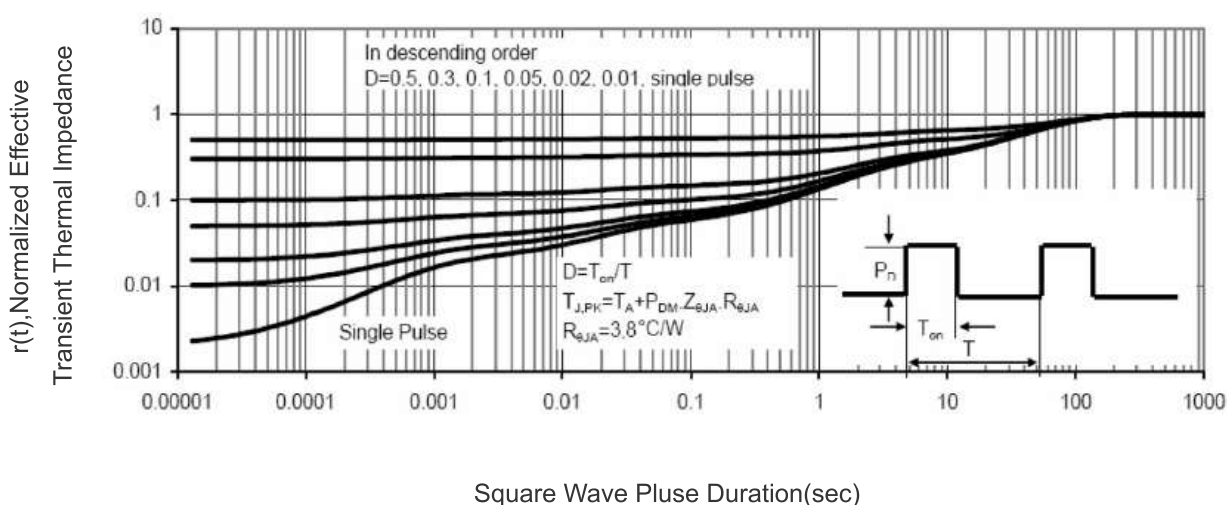
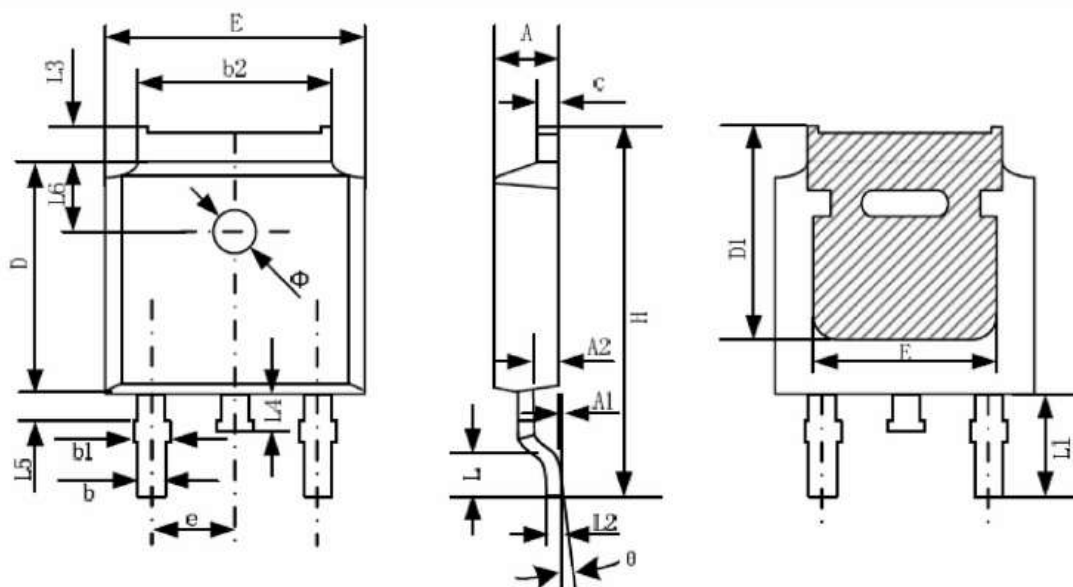


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.20	2.38	0.087	0.094
A1	0.00	0.10	0.000	0.004
A2	0.90	1.10	0.035	0.043
b	0.72	0.85	0.028	0.033
b1	0.72	0.90	0.028	0.035
b2	5.13	5.46	0.202	0.215
c	0.47	0.60	0.019	0.024
D	6.00	6.20	0.236	0.244
D1	5.25	--	0.207	--
E	6.50	6.70	0.256	0.264
E1	4.70	--	0.185	--
e	2.19	2.39	0.086	0.094
H	9.80	10.40	0.386	0.409
L	1.40	1.70	0.055	0.067
L1	2.90 REF		0.114 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.90	1.25	0.035	0.049
L4	0.60	1.00	0.024	0.039
L5	0.15	0.75	0.006	0.030
L6	1.80 REF		0.071 REF	
Φ	1.20	1.40	0.047	0.055
θ	0°	8°	0°	8°

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