MJ N-Channel Enhancement Mode Power MOSFET

Description

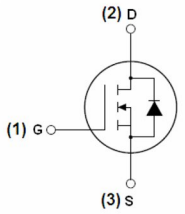
The MJ15H10TA uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

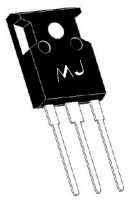
- V_{DS}=150V,I_D=100A
  $R_{DS(ON)}$<11mΩ @ V_{GS}=10V (Typ:9.5mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Special designed for convertors and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



TO-247 top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ15H10TA	MJ15H10TA	TO-247	-	-	-

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous(T_C =100℃)	$I_{D(100℃)}$	70	A
Pulsed Drain Current	I_{DM}	390	A
Maximum Power Dissipation	P_D	370	W
Single pulse avalanche energy (Note 3)	E_{AS}	1600	mJ
Derating factor		2.47	W/℃
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 1)	$R_{\theta JA}$	0.41	℃/W

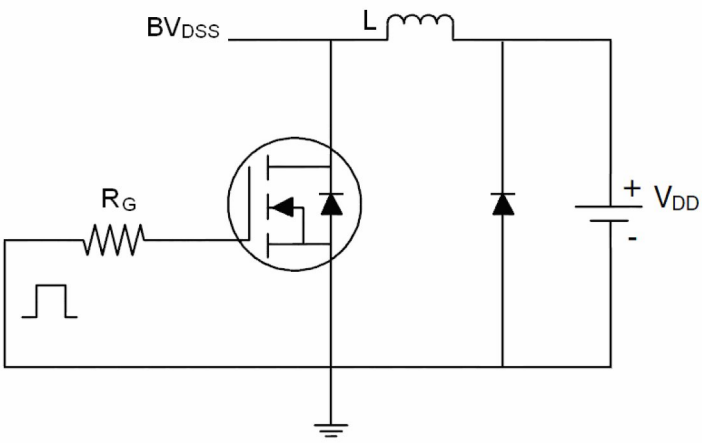
Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} ,I_D=250μA	2.5	3.7	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	9.5	11	mΩ
Forward Transconductance	g_{FS}	V_{DS}=25V,I_D=40A	100	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz	-	7500	-	PF
Output Capacitance	C_{oss}		-	640	-	PF
Reverse Transfer Capacitance	C_{rss}		-	426	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=75V,I_D=2A,R_L=15Ω ,R_G=2.5Ω,V_{GS}=10V	-	32.5	-	nS
Turn-on Rise Time	t_r		-	30	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	113	-	nS
Turn-Off Fall Time	t_f		-	48	-	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=40A, V_{GS}=10V	-	138	-	nC
Gate-Source Charge	Q_{gs}		-	46	-	nC
Gate-Drain Charge	Q_{gd}		-	39	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=40A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	100	A
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=40A di/dt=100A/μs (Note 3)	-	45	-	nS
Reverse Recovery Charge	Q_{rr}		-	80	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

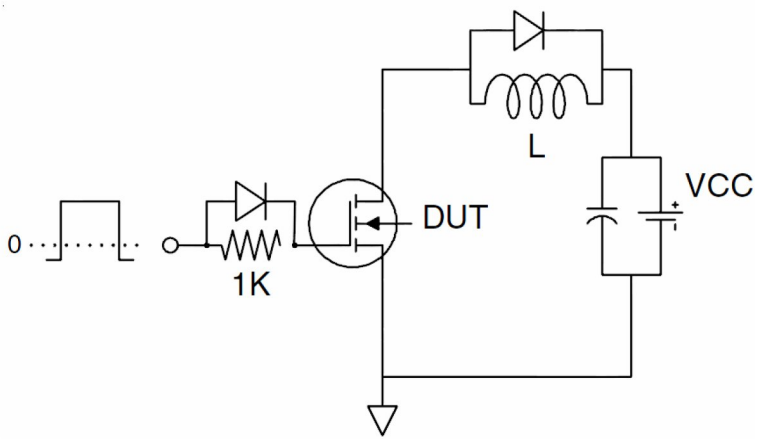
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t≤10sec.
③ Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition：Tj=25℃,V_{DD}=40V,V_G=10V,L=0.5mH,Rg=25Ω

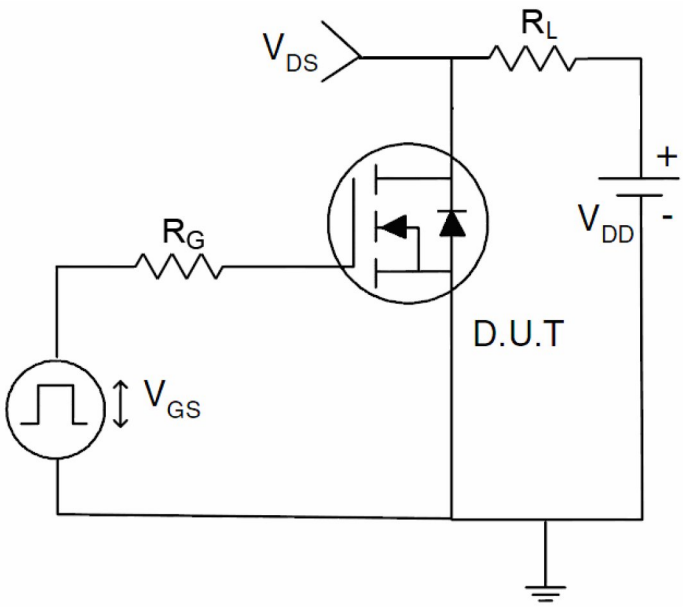
Test circuit



EAS test Circuit

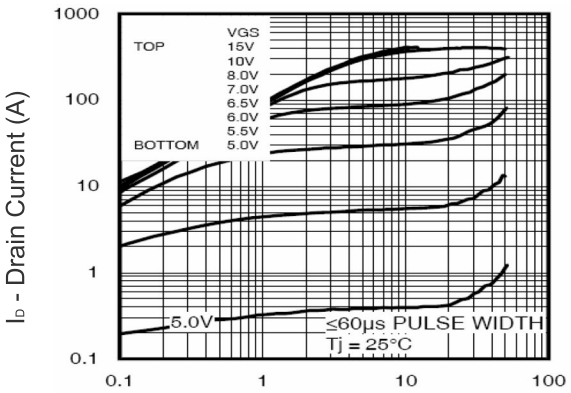


Gate charge test Circuit



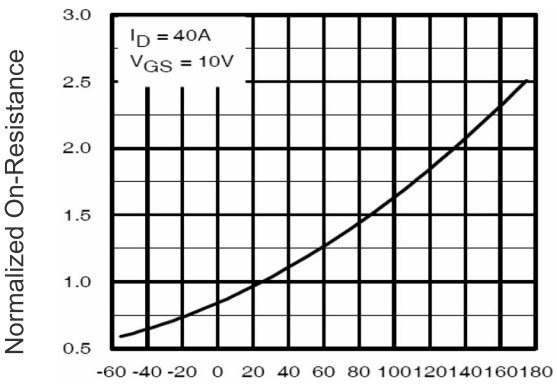
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



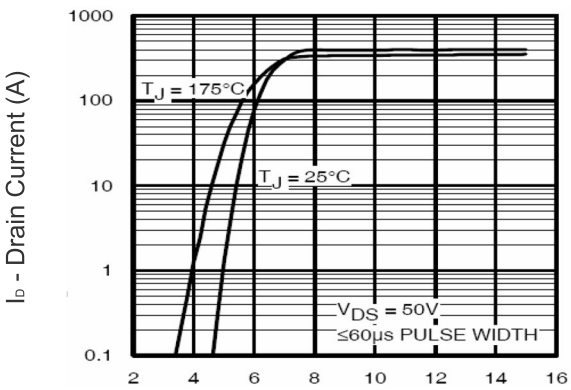
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



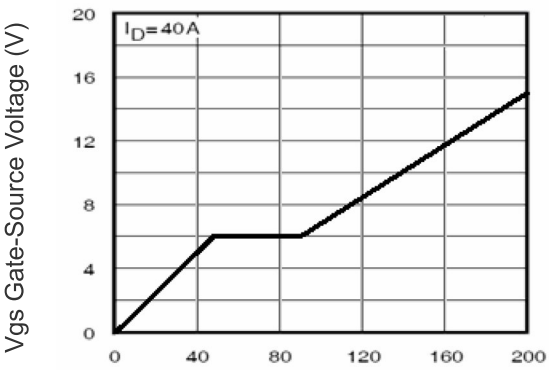
TJ -Junction Temperature(℃)

Figure 4 Rdson-Junction Temperature



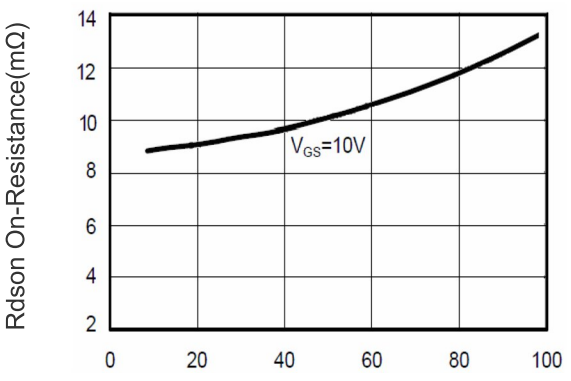
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



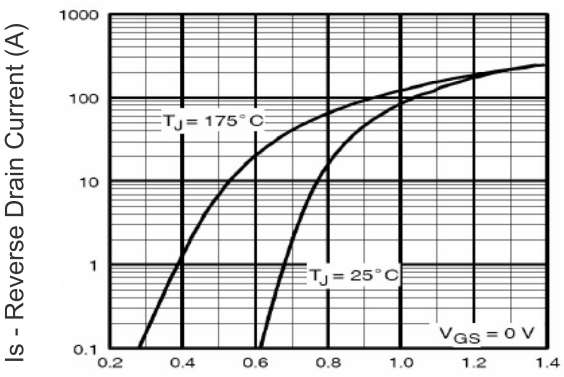
Qg Gate Charge (nC)

Figure 5 Gate Charge



ID - Drain Current (A)

Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

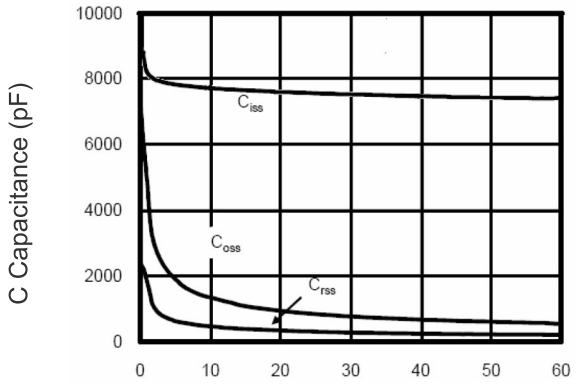


Figure 7 Capacitance vs Vds

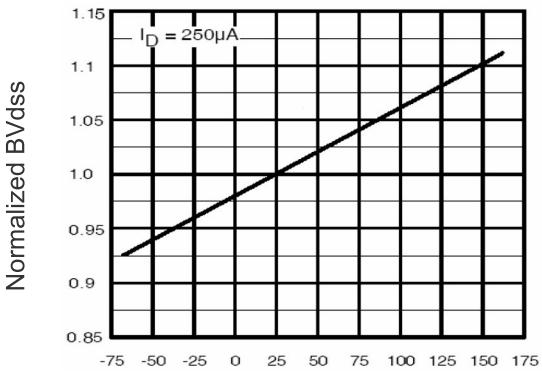


Figure 9 BV_{DSS} vs Junction Temperature

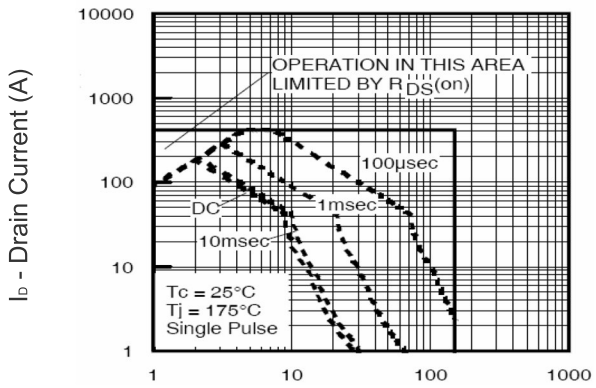


Figure 8 Safe Operation Area

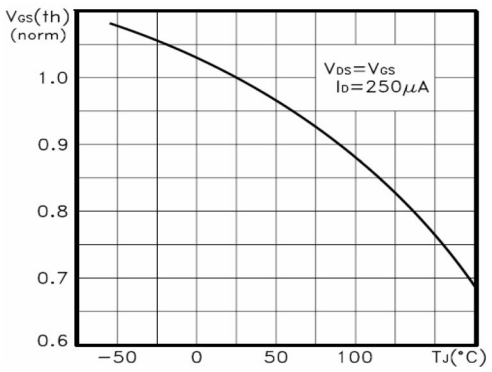


Figure 10 $V_{GS(th)}$ vs Junction Temperature

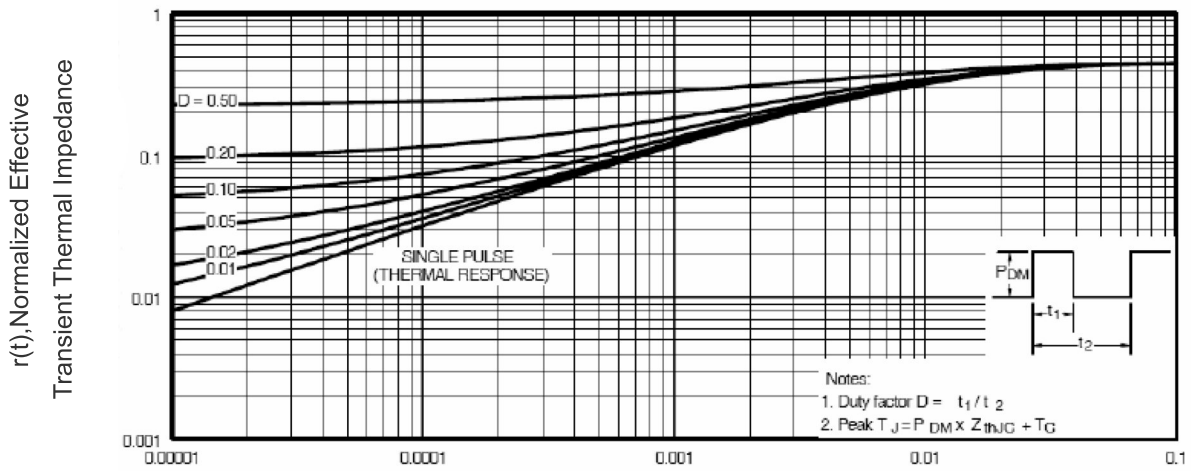
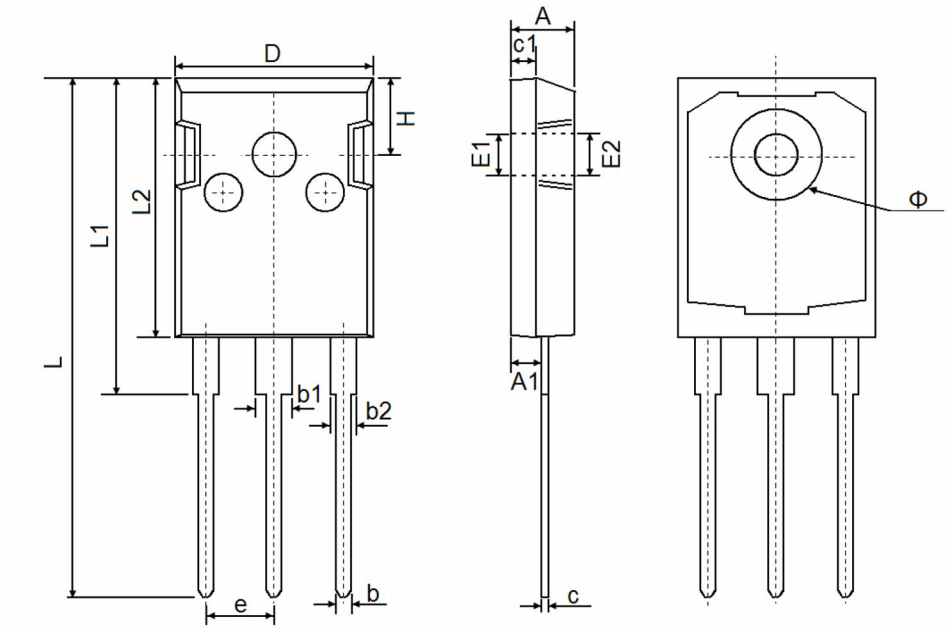


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-247 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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