

MJ N-Channel Enhancement Mode Power MOSFET

Description

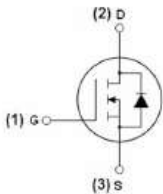
The MJ15H10D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

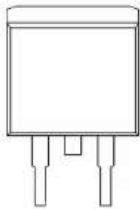
- ◆ $V_{DS} = 150V, I_D = 100A$
 $R_{DS(ON)} < 11m\Omega @ V_{GS} = 10V$ (Typ:9.5m Ω)
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Special designed for convertors and power controls
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

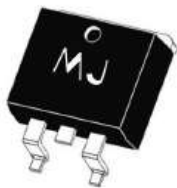
- ◆ Power switching application
- ◆ Hard switched and High frequency circuits
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-263-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ15H10D	MJ15H10D	TO-263-2L	-	-	-

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_C = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	70	A
Pulsed Drain Current	I_{DM}	390	A
Maximum Power Dissipation	P_D	370	W
Derating factor		2.47	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	1600	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.41	°C/W
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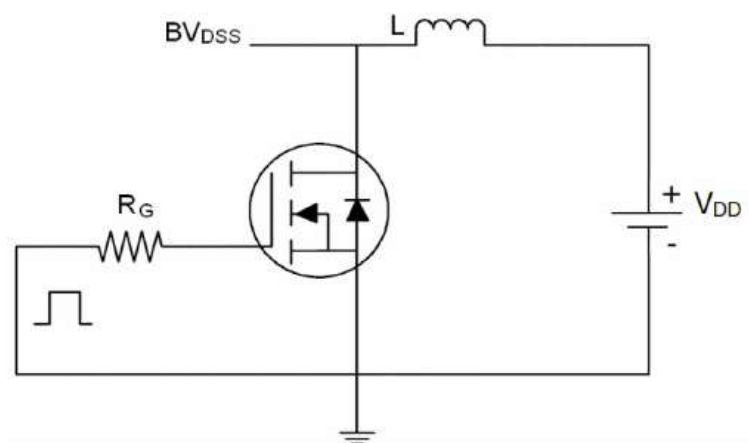
Electrical Characteristics (T_c =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2.5	3.4	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	9.5	11	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V,I _D =40A	100	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V F=1.0MHz	-	7500	-	PF
Output Capacitance	C _{oss}		-	640	-	PF
Reverse Transfer Capacitance	C _{rss}		-	426	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =75V,I _D =2A,R _L =15Ω R _G =2.5Ω,V _{GS} =10V	-	32.5	-	nS
Turn-on Rise Time	t _r		-	30	-	nS
Turn-Off Delay Time	t _{d(off)}		-	113	-	nS
Turn-Off Fall Time	t _f		-	48	-	nS
Total Gate Charge	Q _g	V _{DS} =75V,I _D =40A V _{GS} =10V	-	138	-	nC
Gate-Source Charge	Q _{gs}		-	46	-	nC
Gate-Drain Charge	Q _{gd}		-	39	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =40A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	100	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =40A di/dt=100A/μs ^(Note 3)	-	45	-	nS
Reverse Recovery Charge	Q _{rr}		-	80	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

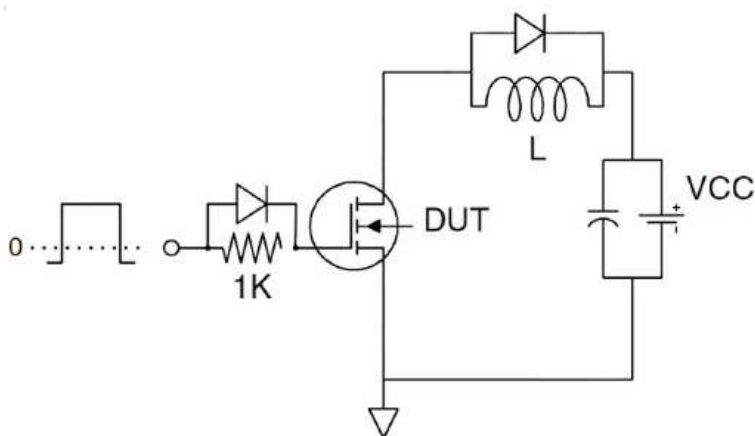
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,R_g=25Ω

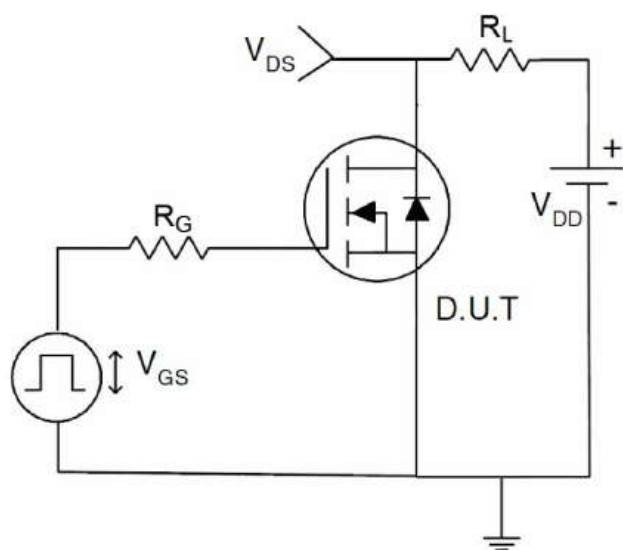
Test circuit



EAS test Circuit

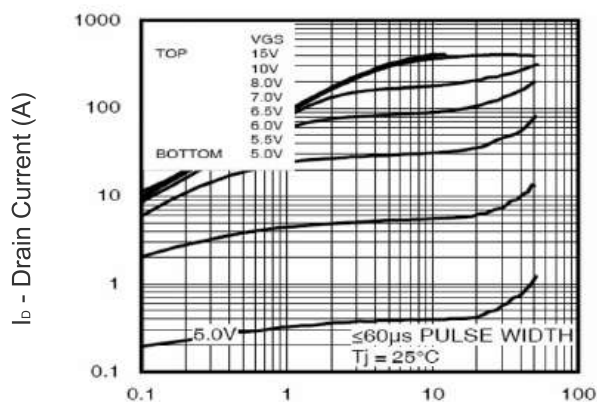


Gate charge test Circuit

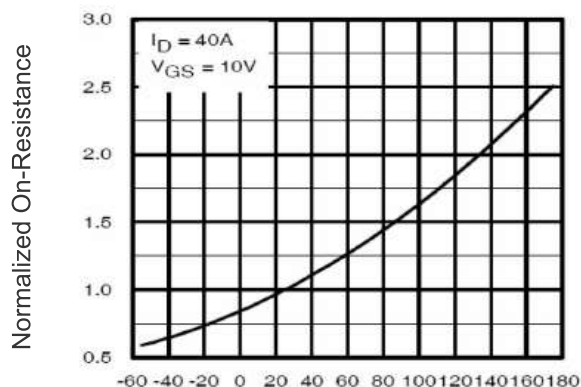


Switch Time Test Circuit

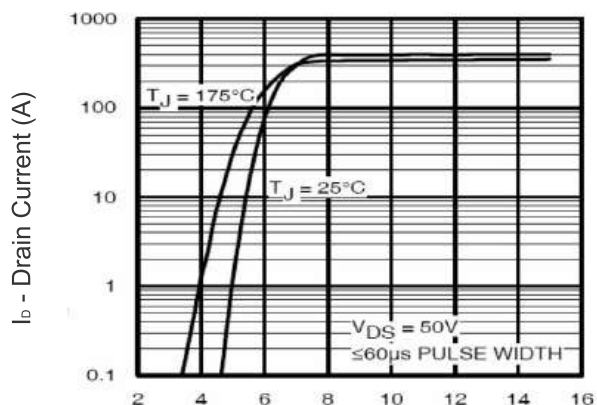
Typical Electrical and Thermal Characteristics (Curves)



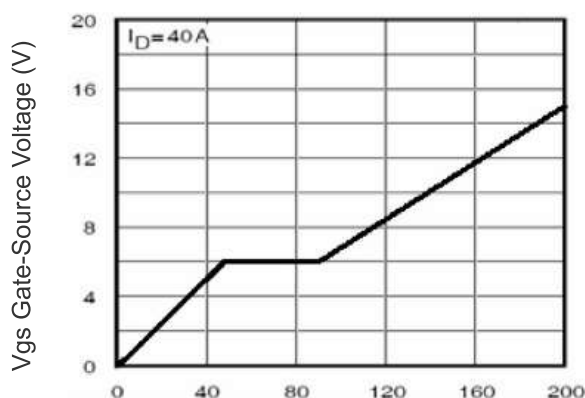
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



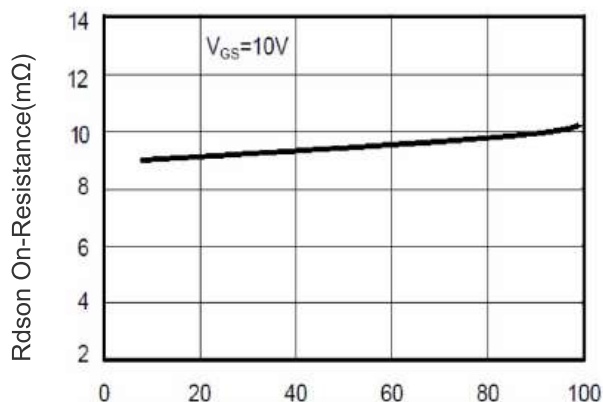
T_J -Junction Temperature($^\circ C$)
Figure 4 Rdson-Junction Temperature



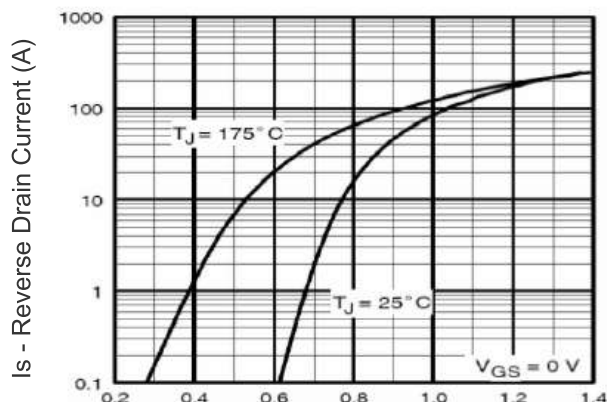
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



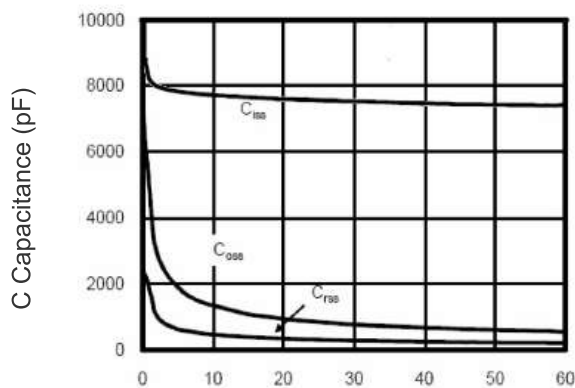
Qg Gate Charge (nC)
Figure 5 Gate Charge



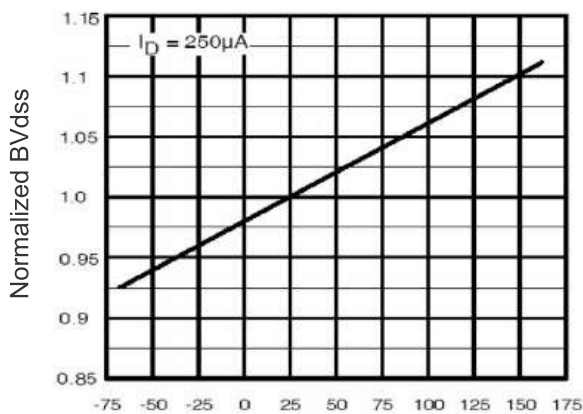
I_D - Drain Current (A)
Figure 3 Rdson- Drain Current



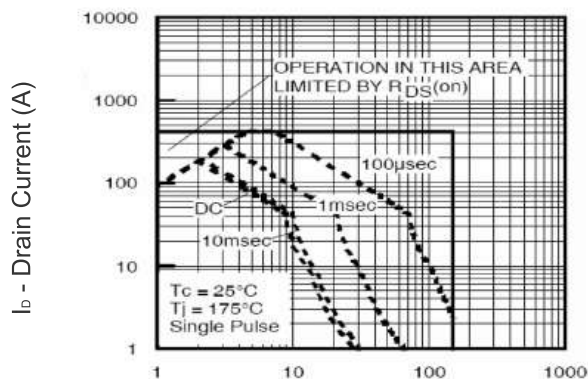
Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



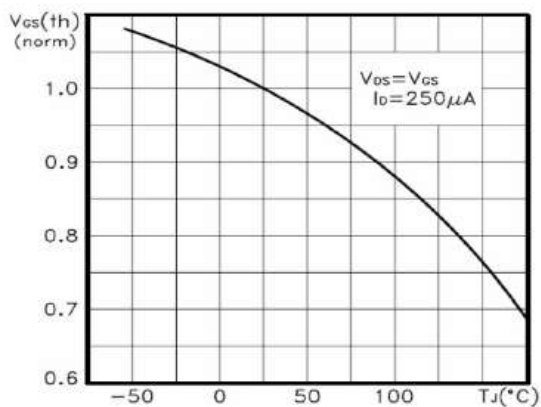
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



Tj -Junction Temperature(°C)
Figure 9 BV_{DSS} vs Junction Temperature



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature

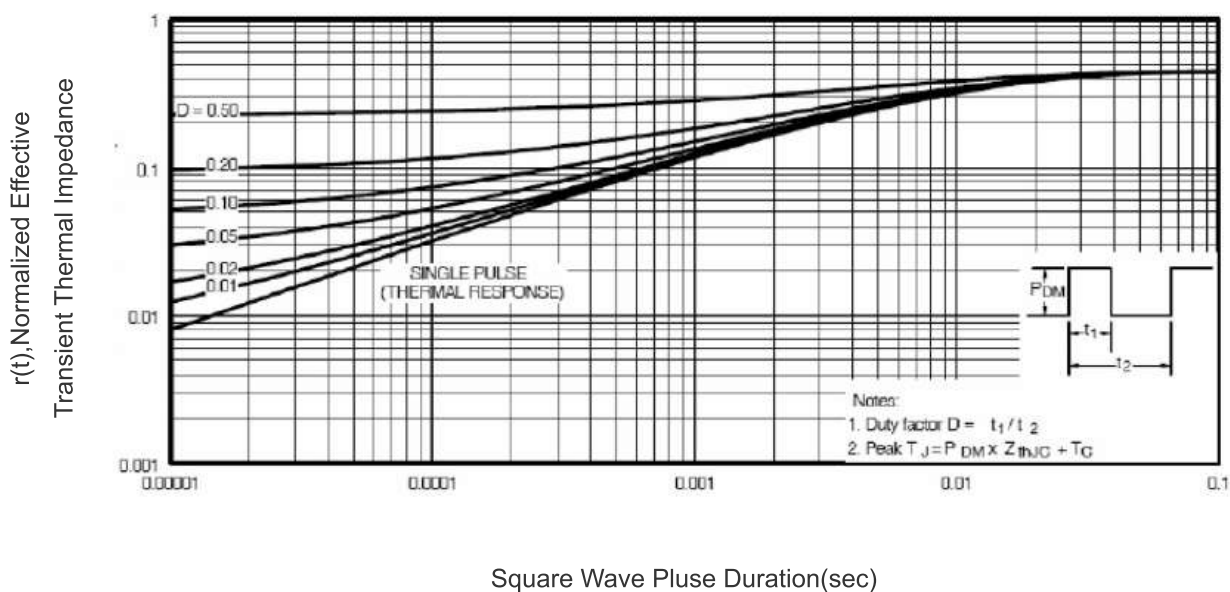
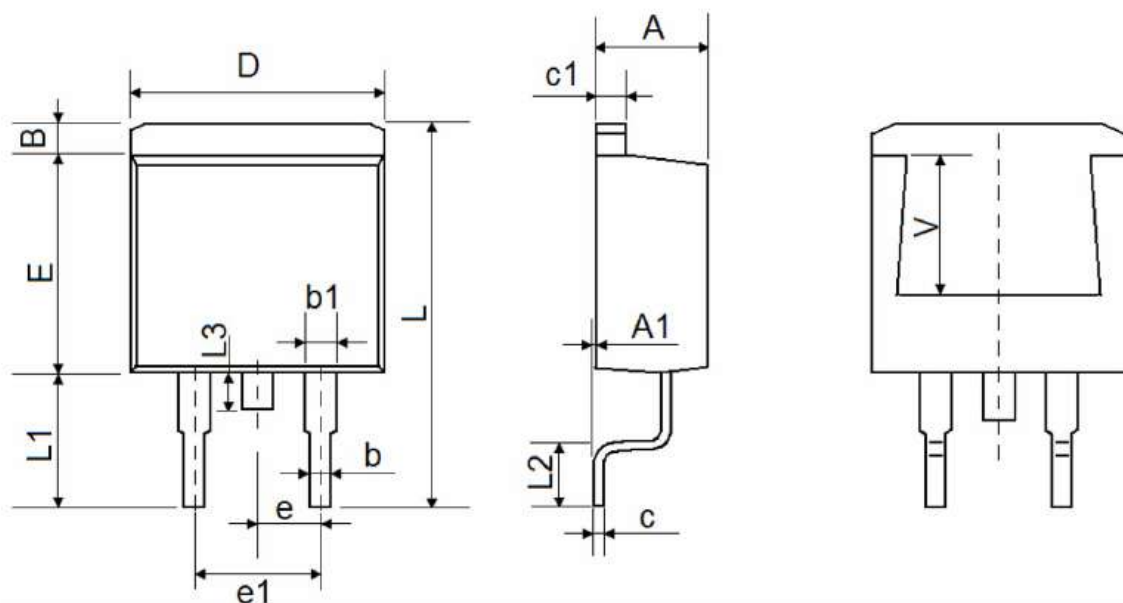


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF		0.220 REF	

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