

MJ N-Channel Enhancement Mode Power MOSFET

Description

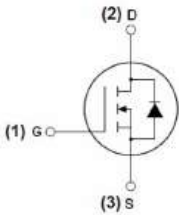
The MJ0224D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

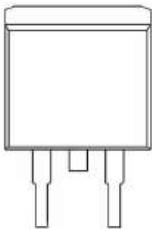
- ◆ $V_{DS} = 200V, I_D = 24A$
 $R_{DS(ON)} < 80m\Omega @ V_{GS} = 10V$ (Typ:64m Ω)
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Good stability and uniformity with high E_{AS}
- ◆ Excellent package for good heat dissipation
- ◆ Special process technology for high ESD capability

Application

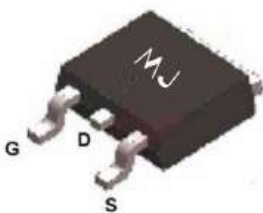
- ◆ Power switching application
- ◆ Hard switched and High frequency circuits
- ◆ Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-263-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ0224D	MJ0224D	TO-263-2L	-	-	-

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	24	A
Drain Current-Continuous($T_C = 100^{\circ}C$)	$I_{D(100^{\circ}C)}$	17	A
Pulsed Drain Current	I_{DM}	100	A
Maximum Power Dissipation	P_D	150	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	250	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1	$^{\circ}C/W$
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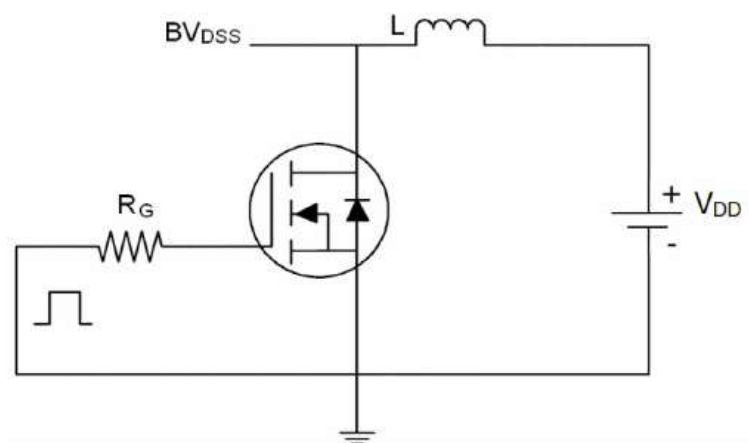
Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	200	220	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =200V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =15A	-	64	80	mΩ
Forward Transconductance	g _{FS}	V _{DS} =50V,I _D =15A	30	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V F=1.0MHz	-	4200	-	PF
Output Capacitance	C _{oss}		-	163	-	PF
Reverse Transfer Capacitance	C _{rss}		-	75	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =100V,I _D =15A V _{GS} =10V,R _{GEN} =2.5Ω	-	10	-	nS
Turn-on Rise Time	t _r		-	18	-	nS
Turn-Off Delay Time	t _{d(off)}		-	22	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =100V,I _D =15A V _{GS} =10V	-	60	-	nC
Gate-Source Charge	Q _{gs}		-	19	-	nC
Gate-Drain Charge	Q _{gd}		-	17	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =11A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	24	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =15A di/dt=100A/μs <small>(Note 3)</small>	-	90	-	nS
Reverse Recovery Charge	Q _{rr}		-	300	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

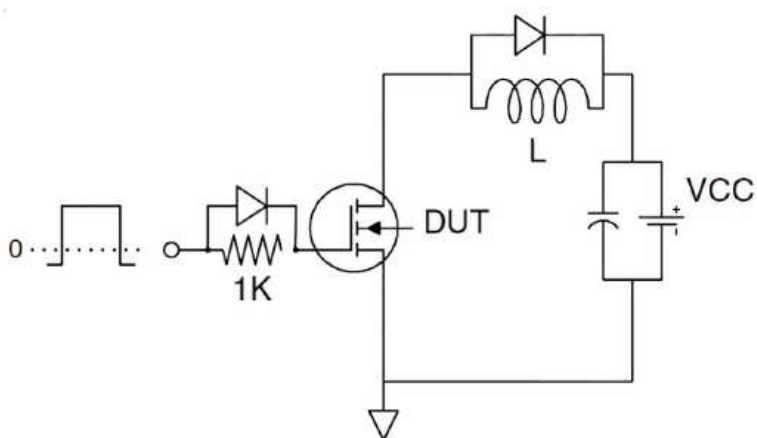
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25°C,V_{DD}=100V,V_G=10V,L=0.5mH,R_g=25Ω

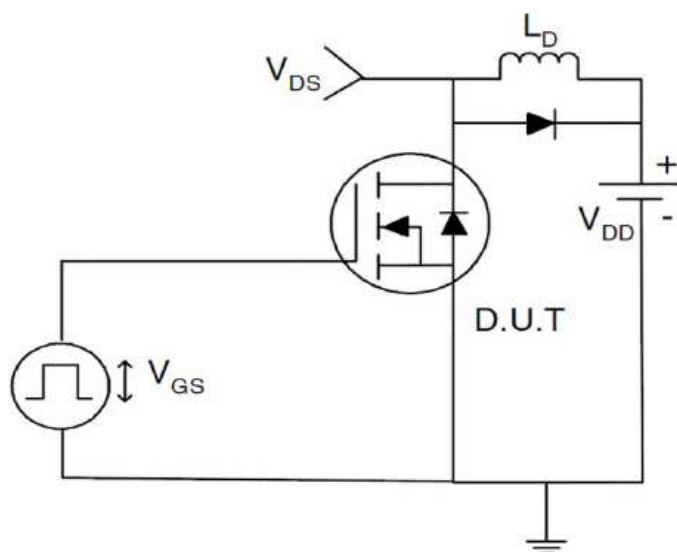
Test circuit



EAS test Circuit

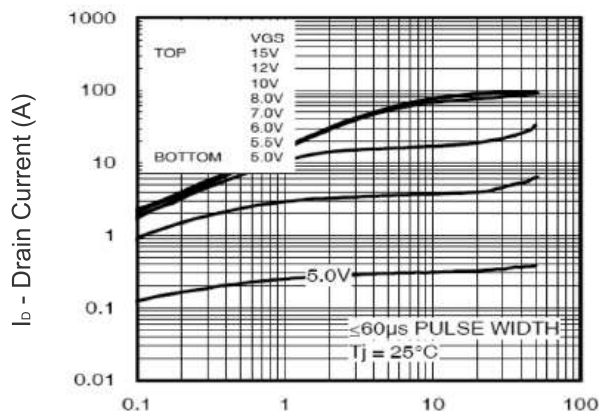


Gate charge test Circuit

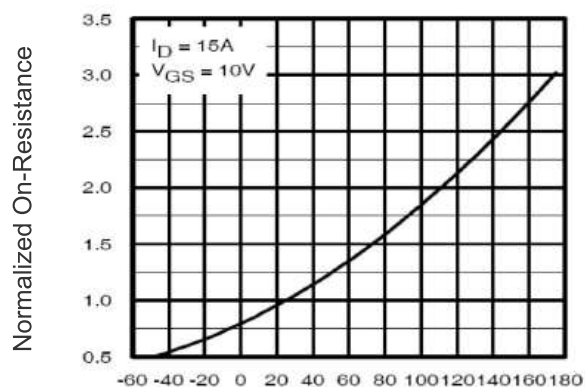


Switch Time Test Circuit

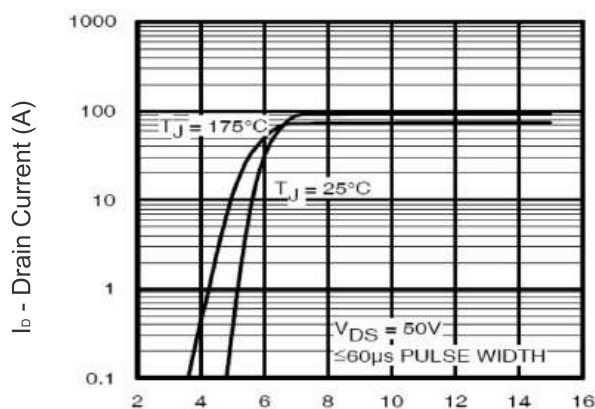
Typical Electrical and Thermal Characteristics (Curves)



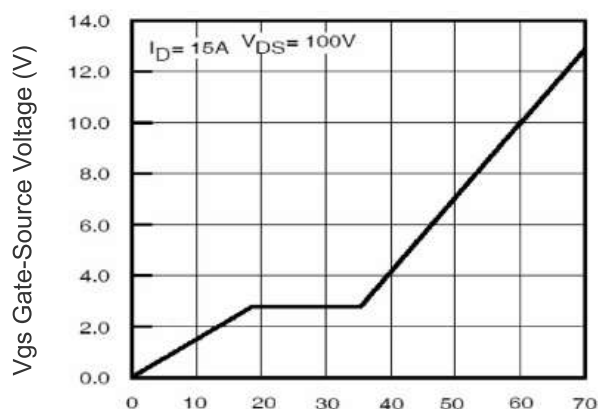
V_{DS} Drain-Source Voltage (V)
Figure 1 Output Characteristics



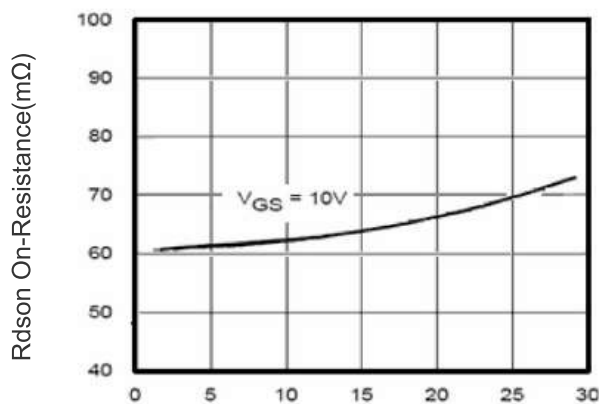
T_J -Junction Temperature($^\circ\text{C}$)
Figure 4 $R_{DS(on)}$ -Junction Temperature



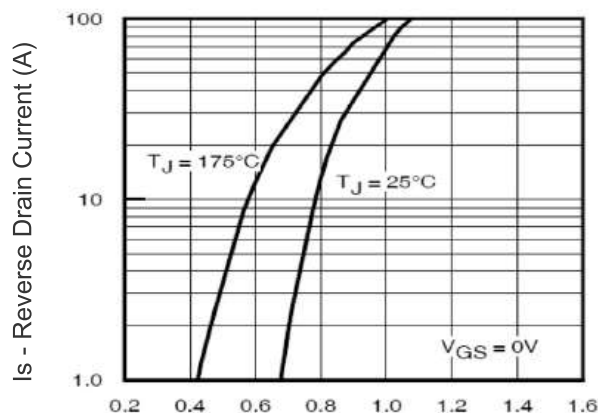
V_{GS} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



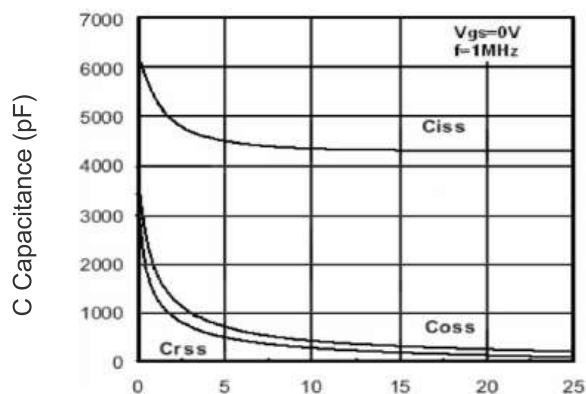
Q_g Gate Charge (nC)
Figure 5 Gate Charge



I_D - Drain Current (A)
Figure 3 $R_{DS(on)}$ - Drain Current

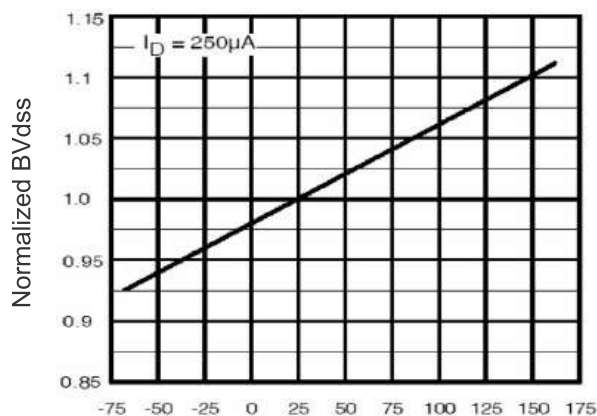


V_{SD} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



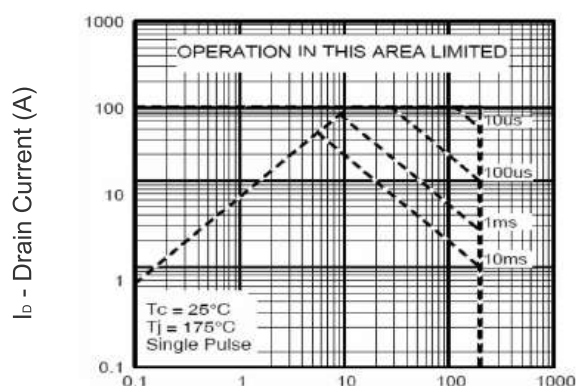
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



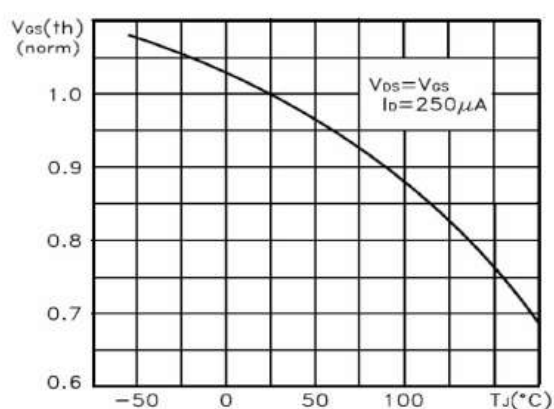
Tj -Junction Temperature(°C)

Figure 9 BV_{DSS} vs Junction Temperature



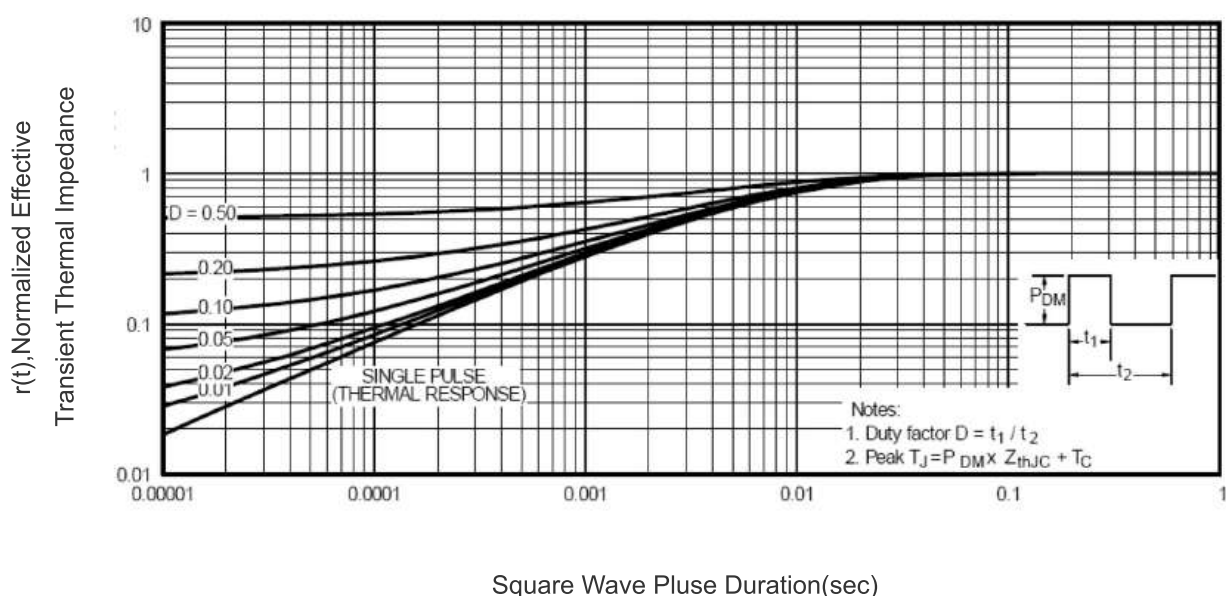
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tj -Junction Temperature(°C)

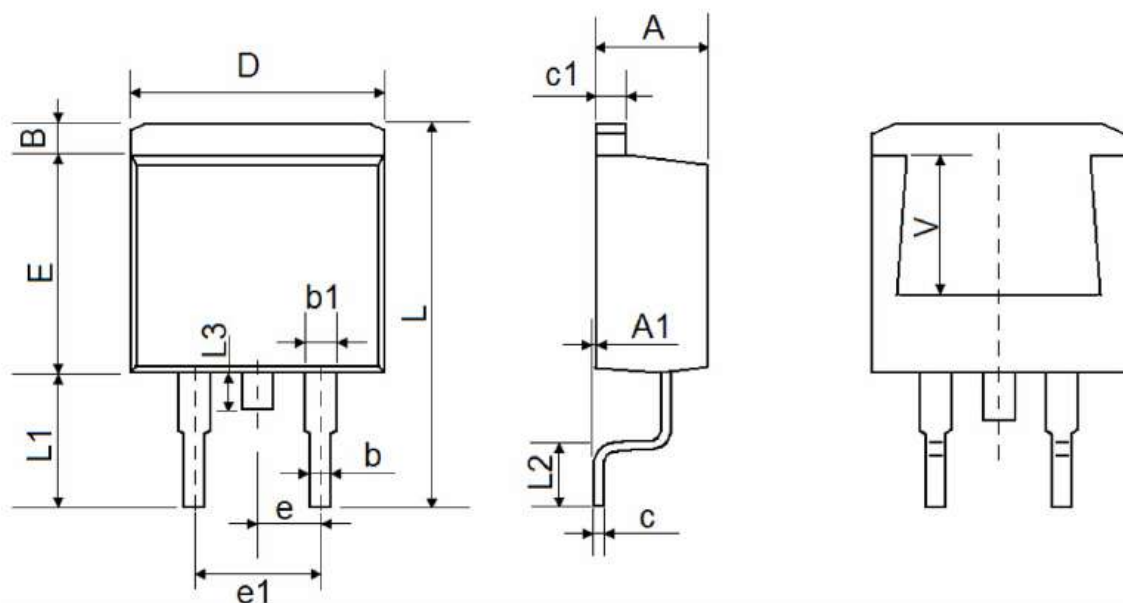
Figure 10 V_{GS(th)} vs Junction Temperature



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF		0.220 REF	

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