

MJ P-Channel Enhancement Mode Power MOSFET

Description

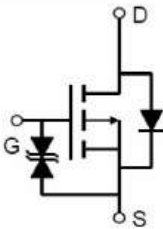
The MJ01P18D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

General Features

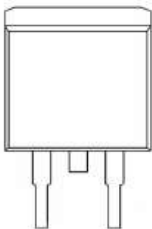
- ◆ $V_{DS} = -100V, I_D = -18A$
 $R_{DS(ON)} < 100m\Omega @ V_{GS} = -10V$ (Typ:85m Ω)
 $R_{DS(ON)} < 120m\Omega @ V_{GS} = -10V$ (Typ:95m Ω)
- ◆ Super high dense cell design
- ◆ Advanced trench process technology
- ◆ Reliable and rugged
- ◆ High density cell design for ultra low On-Resistance

Application

- ◆ Power management in notebook computer
- ◆ Portable equipment and battery powered systems



Schematic diagram



Marking and pin assignment



TO-263-2L top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ01P18D	MJ01P18D	TO-263-2L	-	-	-

Absolute Maximum Ratings (Tc =25 °Cunless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-18	A
Drain Current-Continuous(Tc =100°C)	$I_{D(100^{\circ}C)}$	-12	A
Pulsed Drain Current	I_{DM}	-100	A
Maximum Power Dissipation	P_D	70	W
Derating factor		0.47	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	170	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.14	°C/W
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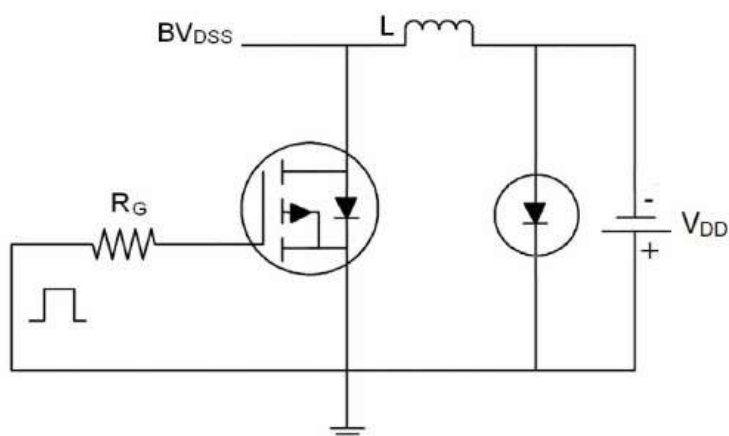
Electrical Characteristics (T_c =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±20	μA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1	-1.9	-3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-16A	-	85	100	mΩ
		V _{GS} =-4.5V, I _D =-16A	-	95	120	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-50V,I _D =-10A	5	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C _{iss}	V _{DS} =-50V,V _{GS} =0V F=1.0MHz	-	3810	-	PF
Output Capacitance	C _{oss}		-	129	-	PF
Reverse Transfer Capacitance	C _{rss}		-	125	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-50V,I _D =-16A V _{GS} =-10V,R _{GEN} =9.1Ω	-	16	-	nS
Turn-on Rise Time	t _r		-	73	-	nS
Turn-Off Delay Time	t _{d(off)}		-	34	-	nS
Turn-Off Fall Time	t _f		-	57	-	nS
Total Gate Charge	Q _g	V _{DS} =-50V,I _D =-16A V _{GS} =-10V	-	70	-	nC
Gate-Source Charge	Q _{gs}		-	12.5	-	nC
Gate-Drain Charge	Q _{gd}		-	15.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V,I _S =-10A	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	-18	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =-16A di/dt=100A/μs <small>(Note 3)</small>	-	88.3	-	nS
Reverse Recovery Charge	Q _{rr}		-	65.9	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

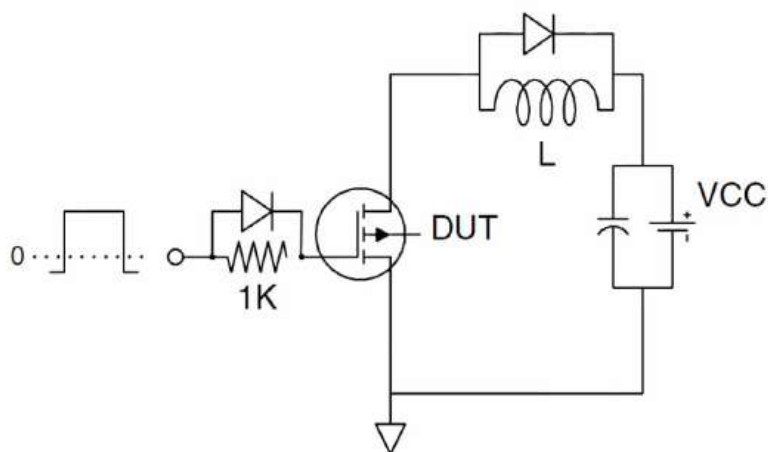
Notes:

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Surface Mounted on FR4 Board, t ≤ 10 sec.
- ③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
- ④ Guaranteed by design, not subject to production
- ⑤ EAS condition: T_J=25℃,V_{DD}=-50V,V_G=-10V,L=0.5mH,R_g=25Ω

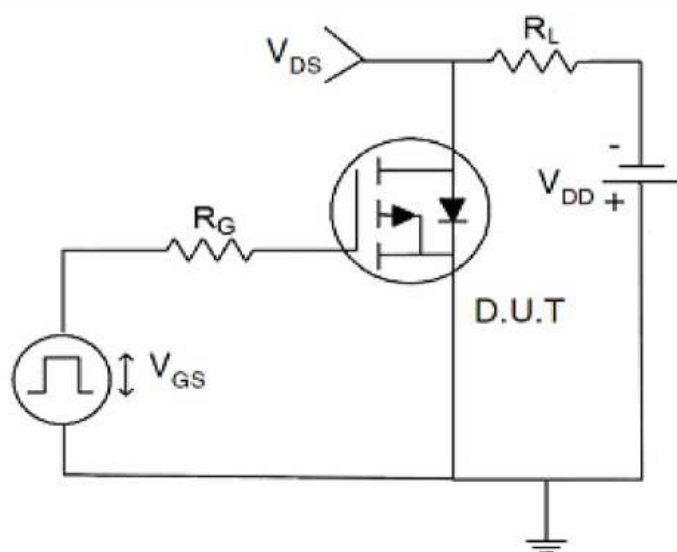
Test circuit



EAS test Circuit

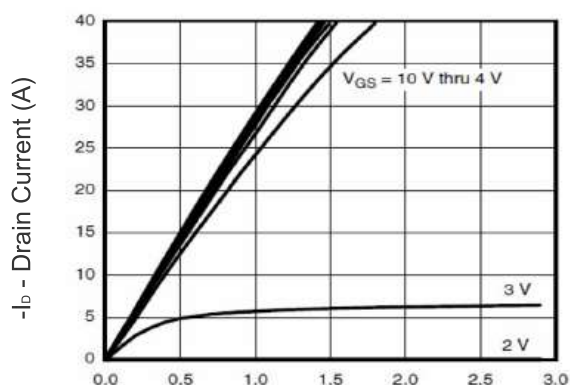


Gate charge test Circuit

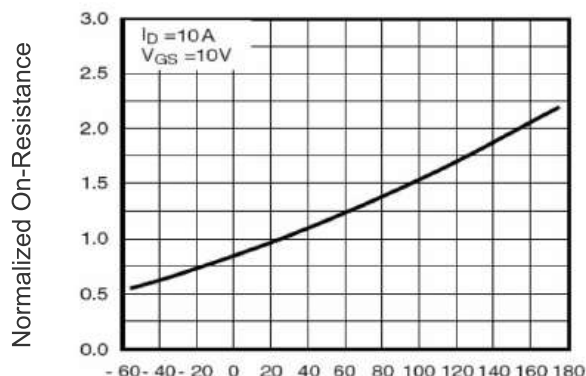


Switch Time Test Circuit

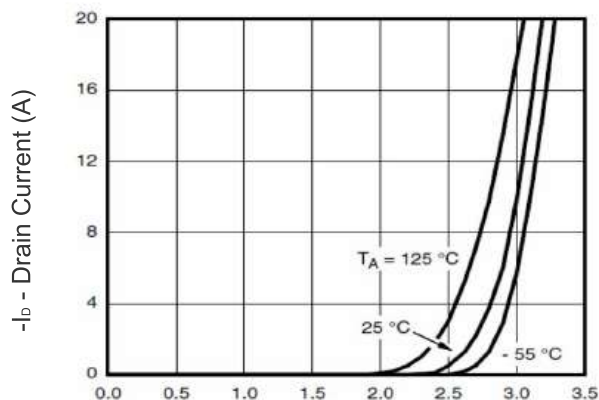
Typical Electrical and Thermal Characteristics (Curves)



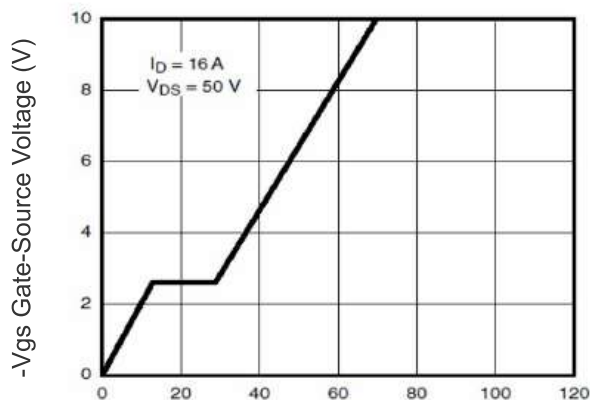
-Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



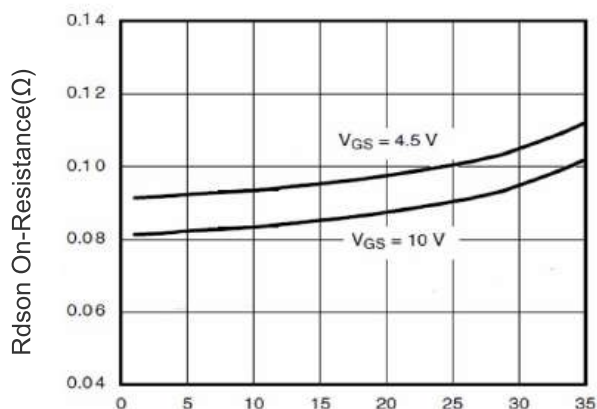
Tj -Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



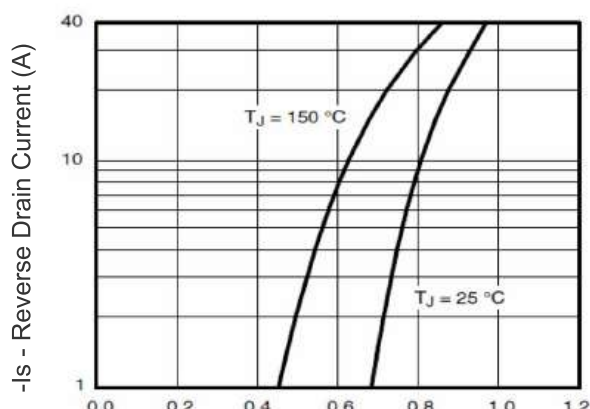
-Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



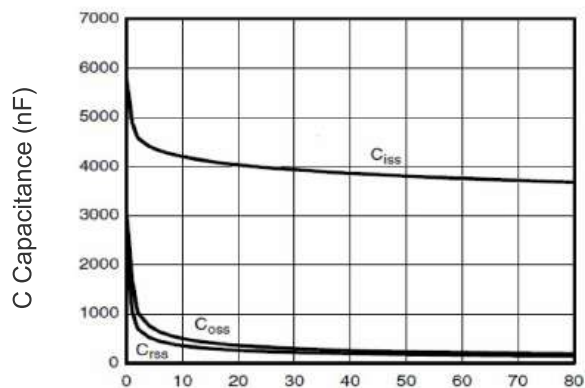
Qg Gate Charge (nC)
Figure 5 Gate Charge



-Id - Drain Current (A)
Figure 3 Rdson- Drain Current

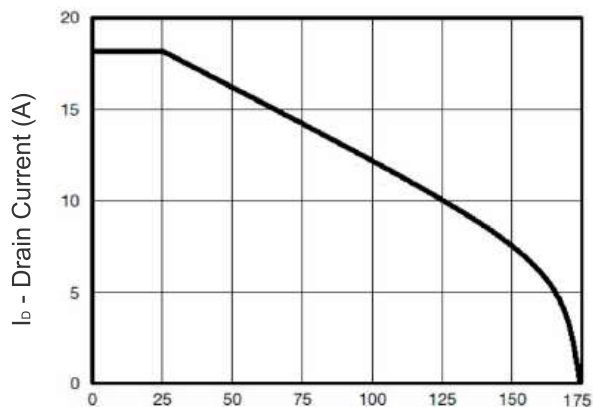


-Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward



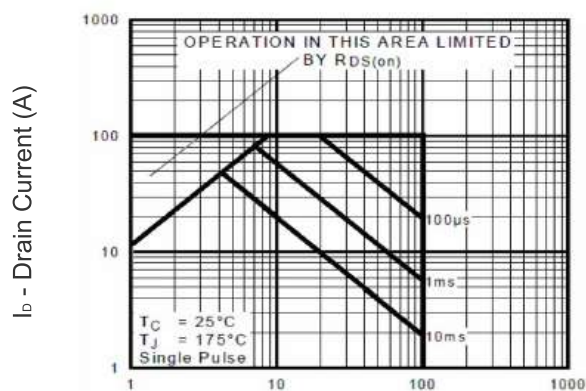
-Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



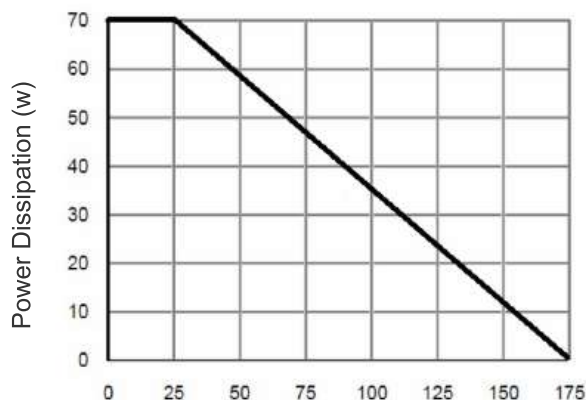
Tc Case Temperature(°C)

Figure 9 Drain Current vs Case Temperature



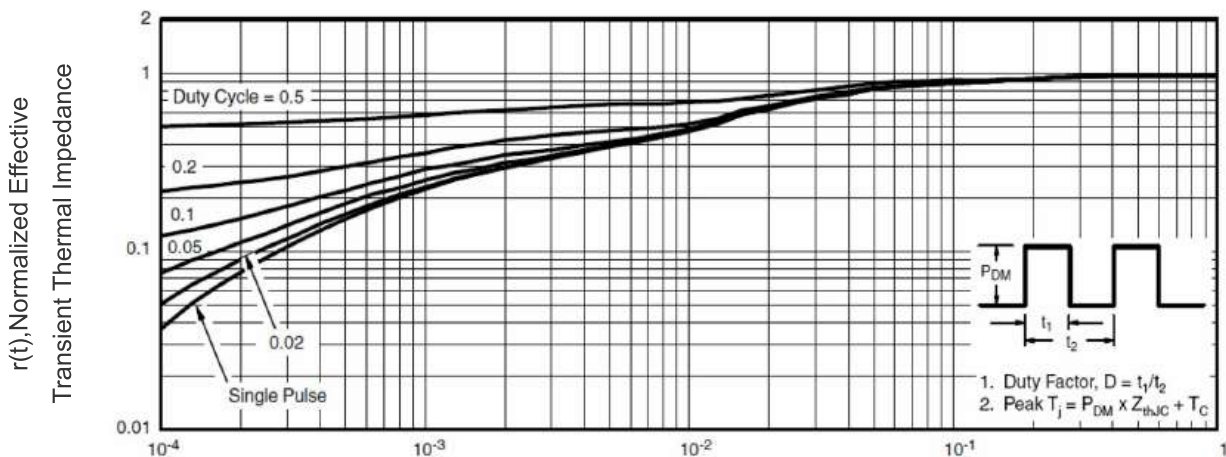
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tc-Case Temperature(°C)

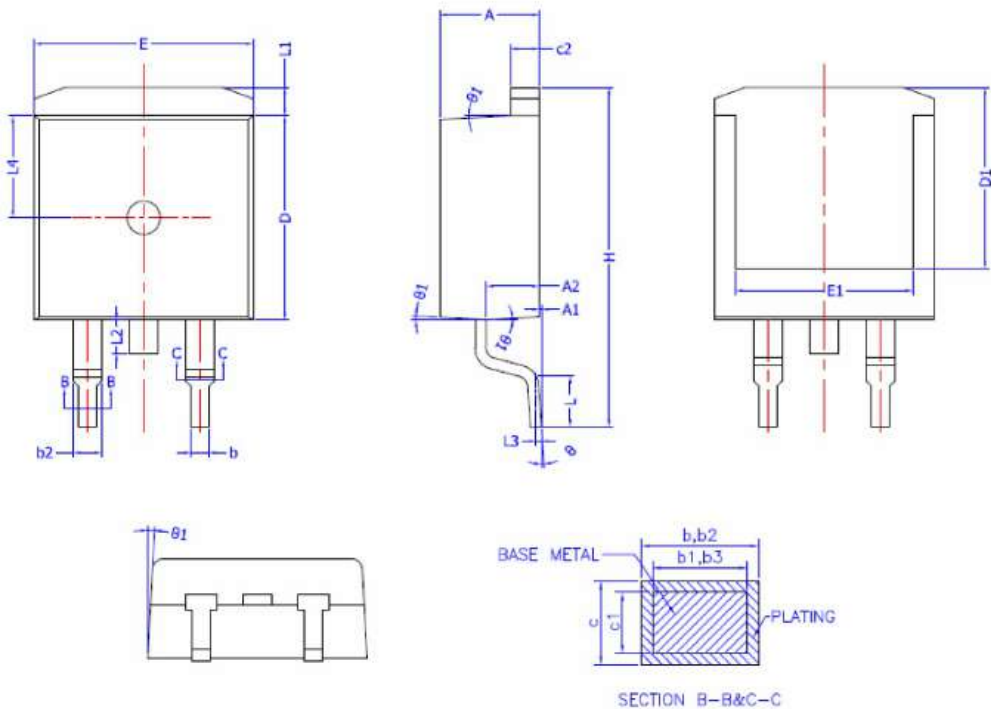
Figure 10 Power De-rating



Square Wave Pluse Duration(sec)

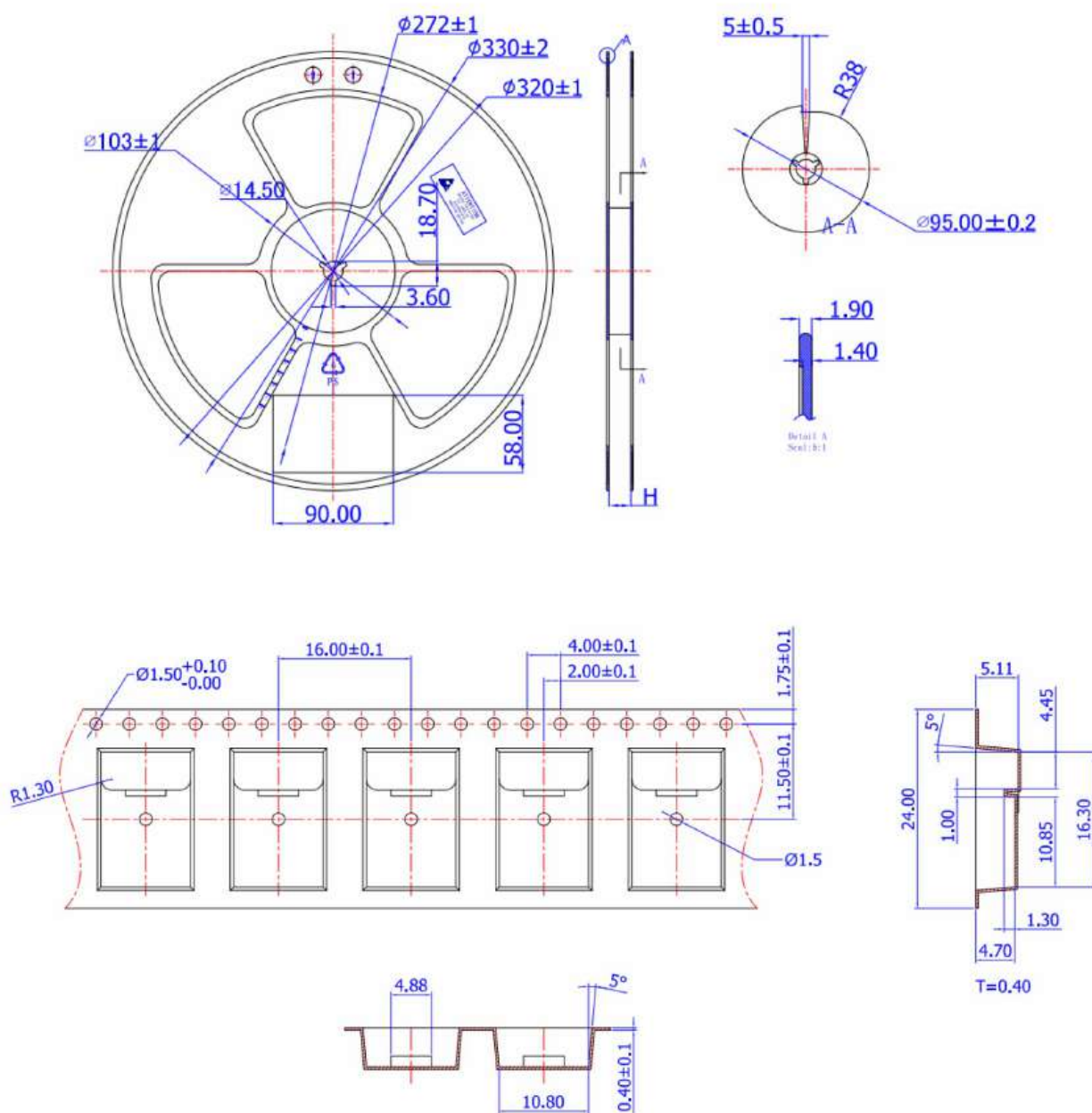
Figure 11 Normalized Maximum Transient Thermal Impedance

TO-263-2L Package Information

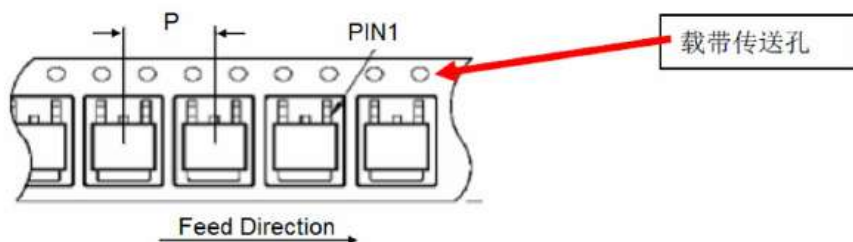


COMMON DIMENSIONS
(UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	0	0.10	0.25
A2	2.20	2.40	2.60
b	0.76	—	0.89
b1	0.75	0.80	0.85
b2	1.23	—	1.37
b3	1.22	1.27	1.32
c	0.47	—	0.60
c1	0.46	0.51	0.56
c2	1.25	1.30	1.35
D	9.10	9.20	9.30
D1	8.00	—	—
E	9.80	9.90	10.00
E1	7.80	—	—
e	2.54 BSC		
H	14.90	15.30	15.70
L	2.00	2.30	2.60
L1	1.17	1.27	1.40
L2	—	—	1.75
L3	0.25BSC		
L4	4.60 REF		
θ	0°	—	8°
θ1	1°	3°	5°



注：产品编入卷盘中时，产品第一支脚(PIN 1)方向朝向载带传送孔。如下图所示。



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