MJ P-Channel Enhancement Mode Power MOSFET

Description

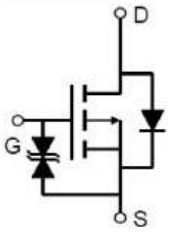
The MJ01P05S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protested.

General Features

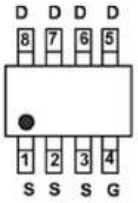
- V_{DS} =-100V,I_D =-5A
  $R_{DS(ON)}$ <100mΩ @ V_{GS}=-10V (Typ:85mΩ)
  $R_{DS(ON)}$ <120mΩ @ V_{GS}=-10V (Typ:95mΩ)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density celldesign for ultra low on-resistance

Application

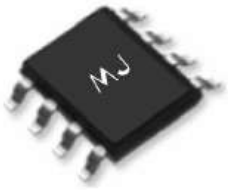
- Power switch
- DC/DC converters



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ01P05S	MJ01P05S	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-5	A
Drain Current-Continuous(T_C =100℃)	$I_{D(100℃)}$	-3.5	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	40	℃/W

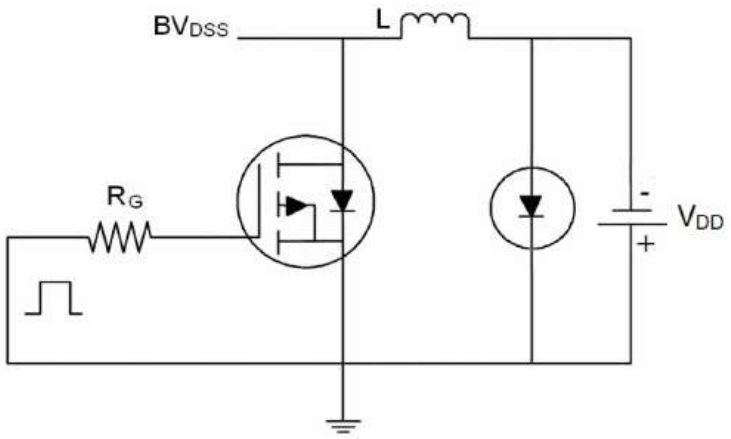
Electrical Characteristics (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS}=±20V,V_{DS}=0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-1.9	-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-5A	-	85	100	mΩ
		V_{GS}=-4.5V, I_D=-5A		95	120	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-5A	5	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=-50V,V_{GS}=0V F=1.0MHz	-	3810	-	PF
Output Capacitance	C_{oss}		-	129	-	PF
Reverse Transfer Capacitance	C_{rss}		-	125	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-50V,I_D=-5A V_{GS}=-10V,R_{GEN}=9Ω	-	16	-	nS
Turn-on Rise Time	t_r		-	73	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	nS
Turn-Off Fall Time	t_f		-	57	-	nS
Total Gate Charge	Q_g	V_{DS}=-50V,I_D=-5A V_{GS}=-10V	-	70	-	nC
Gate-Source Charge	Q_{gs}		-	12.5	-	nC
Gate-Drain Charge	Q_{gd}		-	15.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-5A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-5	A
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=-5A di/dt=100A/μs (Note 3)	-	88.3	-	nS
Reverse Recovery Charge	Q_{rr}		-	65.9	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

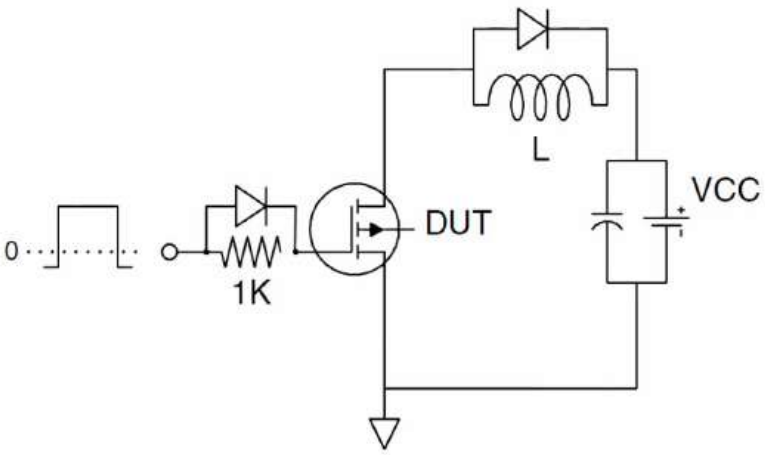
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production
⑤ EAS condition: Tj=25℃,V_{DD}=-50V,V_G=-10V,L=0.5mH,Rg=25Ω

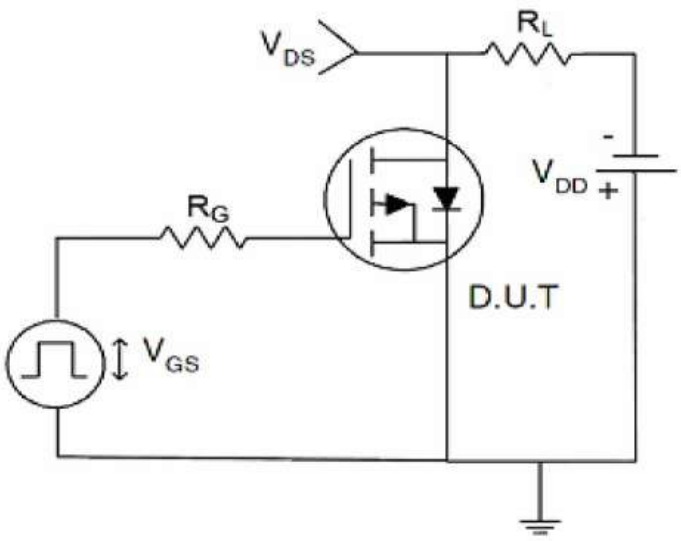
Test circuit



EAS test Circuit

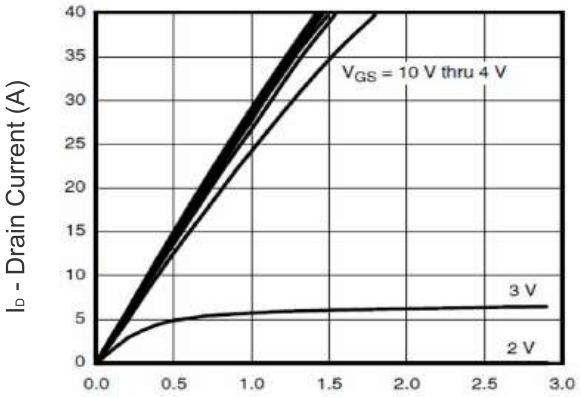


Gate charge test Circuit



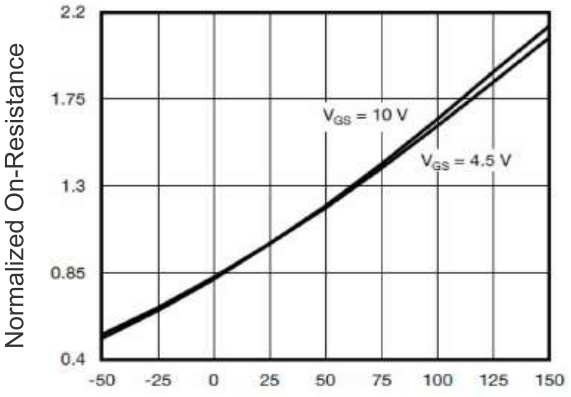
Switch Time Test Circuit

Typical Electrical and Thermal Characteristics (Curves)



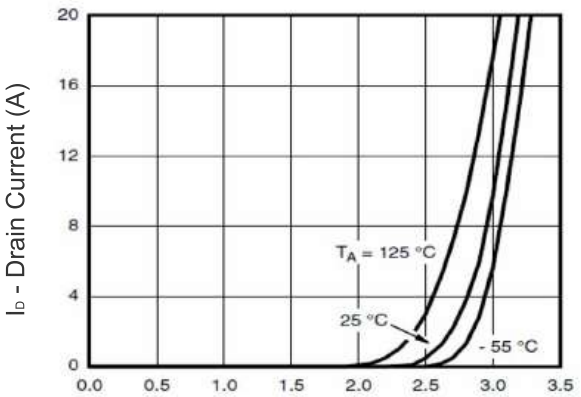
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



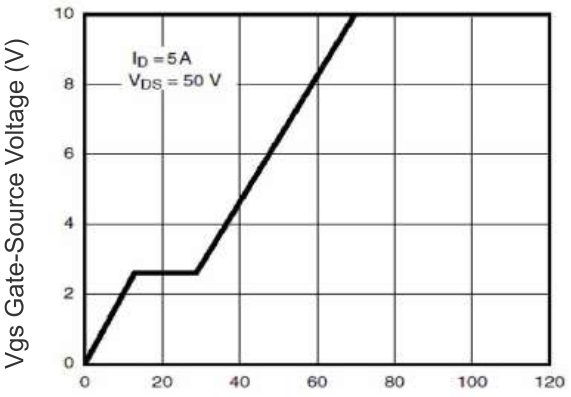
T_J -Junction Temperature(℃)

Figure 4 Rdson-Junction Temperature



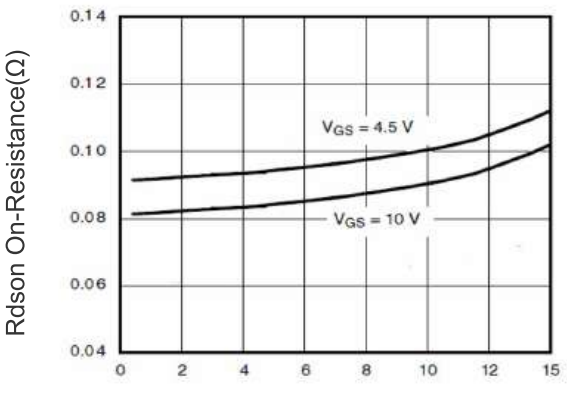
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



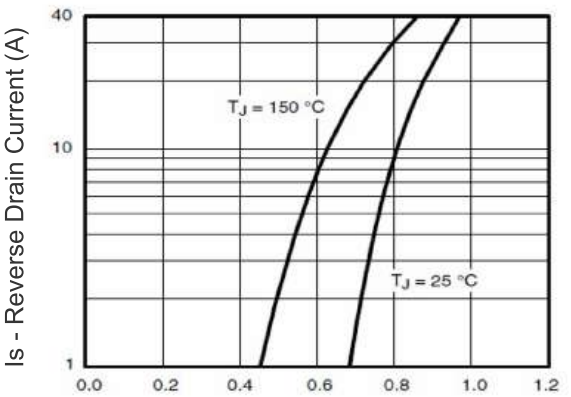
Qg Gate Charge (nC)

Figure 5 Gate Charge



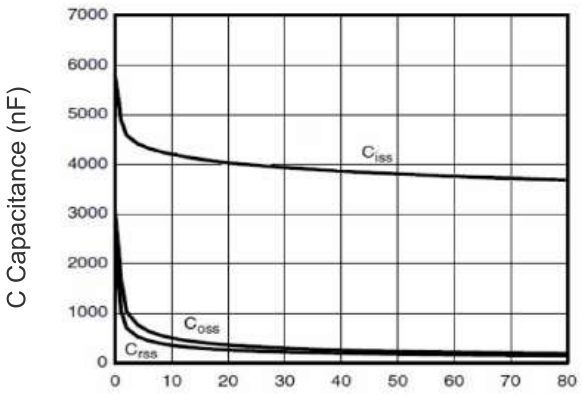
I_D - Drain Current (A)

Figure 3 Rdson- Drain Current



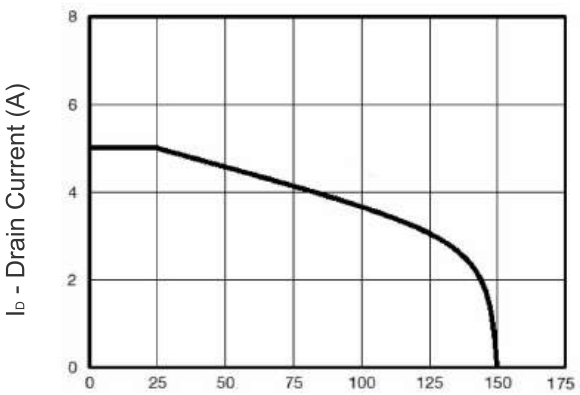
Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward



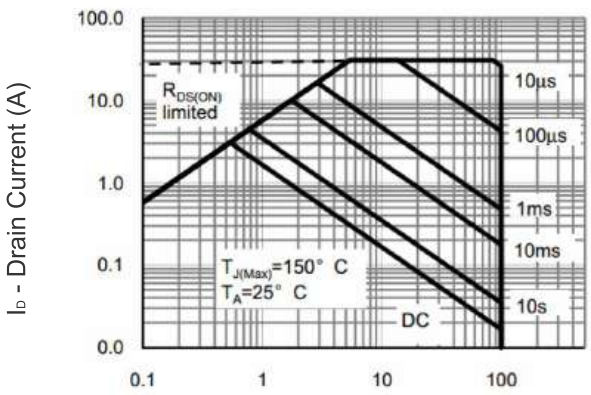
Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds



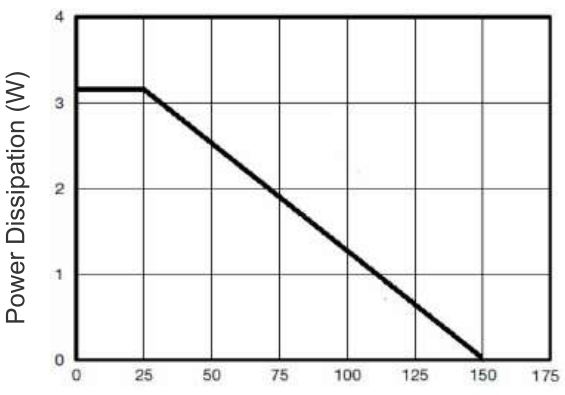
Tc Case Temperature(℃)

Figure 9 Drain Current vs Case Temperature



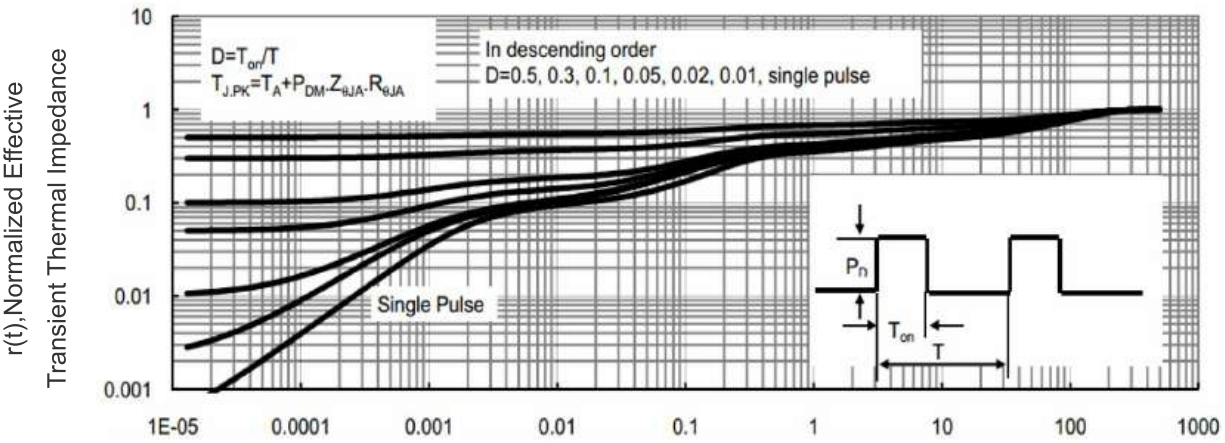
Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



Tc Case Temperature(℃)

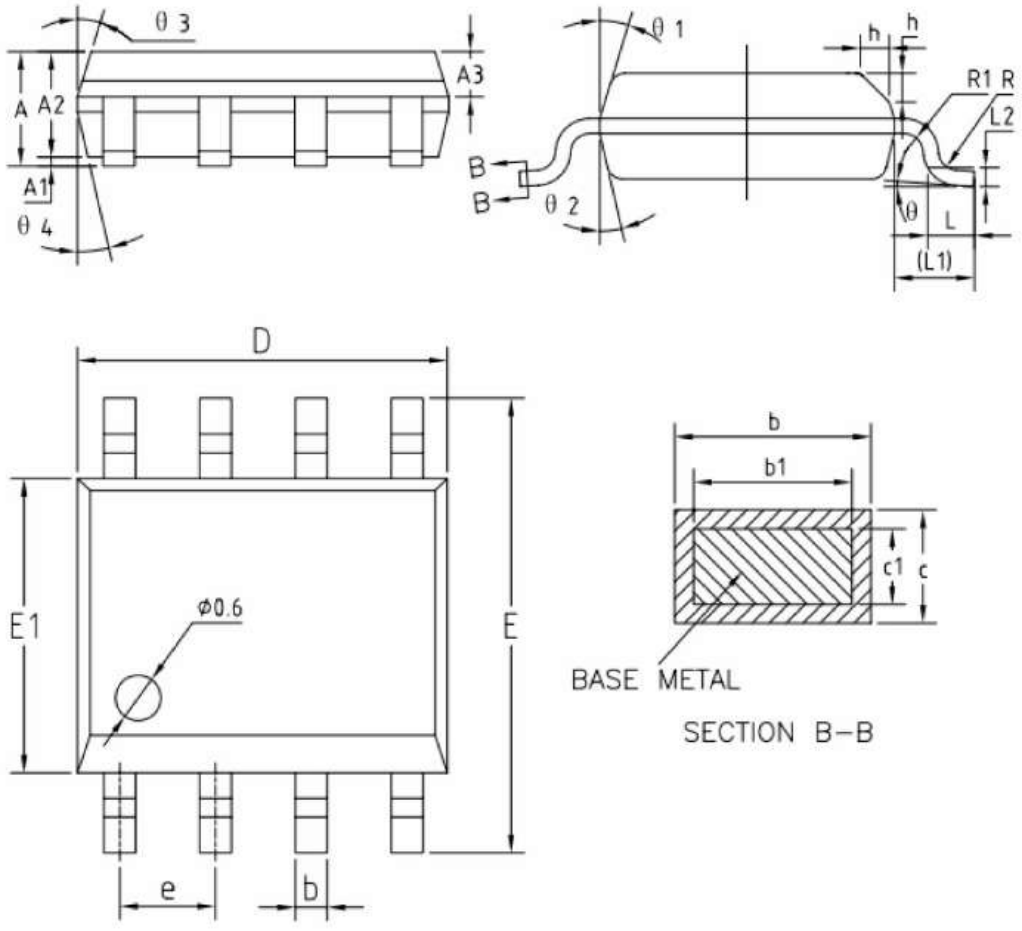
Figure 10 Power De-rating



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.18	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°

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