

MJ N-Channel Enhancement Mode Power MOSFET

Description

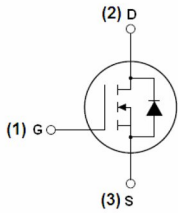
The MJ01H21TC uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

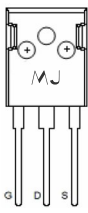
- ◆ $V_{DS}=100V, I_D=210A$
 $R_{DS(ON)}<4.2m\Omega$ @ $V_{GS}=10V$ (Typ3.3m Ω)
- ◆ Good stability and uniformity with high E_{AS}
- ◆ High density cell design for ultra low R_{dson}
- ◆ Fully characterized avalanche voltage and current
- ◆ Excellent package for good heat dissipation

Application

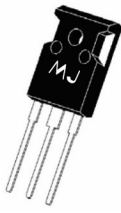
- ◆ DC motor drive
- ◆ High efficiency synchronous rectification in SMPS
- ◆ Uninterruptible power supply
- ◆ High speed power switching
- ◆ Hard switched and high frequency circuits



Schematic diagram



Marking and pin assignment



TO-247 top view

100% UIS TESTED! 100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MJ01H21TC	MJ01H21TC	TO-247	-	-	-

Absolute Maximum Ratings ($T_c=25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous($T_c=100^{\circ}\text{C}$)	$I_{D(100^{\circ}\text{C})}$	140	A
Pulsed Drain Current	I_{DM}	850	A
Maximum Power Dissipation	P_D	385	W
Single pulse avalanche energy ^(Note 3)	E_{AS}	2300	mJ
Derating factor		2.57	W/ $^{\circ}\text{C}$
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	13	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}\text{C}$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 4)	$R_{\theta JA}$	0.39	$^{\circ}\text{C/W}$
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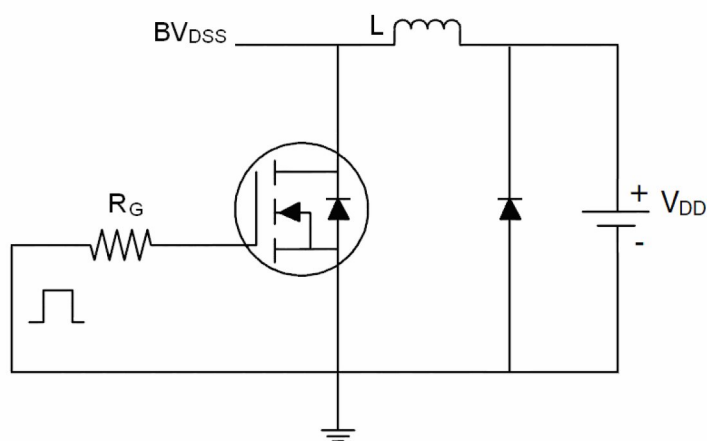
Electrical Characteristics (T_A =25°Cunless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{DS} =±20V,V _{GS} =0V	-	-	±200	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2.5	3.5	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	3.3	4.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =25V,I _D =40A	300	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V, F=1.0MHz	-	13500	-	PF
Output Capacitance	C _{oss}		-	862	-	PF
Reverse Transfer Capacitance	C _{rss}		-	659	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V,I _D =2A V _{GS} =10V,R _{GEN} =2.5Ω ^(Note2)	-	68	-	nS
Turn-on Rise Time	t _r		-	45	-	nS
Turn-Off Delay Time	t _{d(off)}		-	215	-	nS
Turn-Off Fall Time	t _f		-	56	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =30A, V _{GS} =10V ^(Note2)	-	304	-	nC
Gate-Source Charge	Q _{gs}		-	64	-	nC
Gate-Drain Charge	Q _{gd}		-	95	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V,I _S =40A	-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F =75A di/dt=100A/μs ^(Note 2)	-	65	-	nS
Reverse Recovery Charge	Q _{rr}		-	98	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible(turn-on is dominated by LS+LD)				

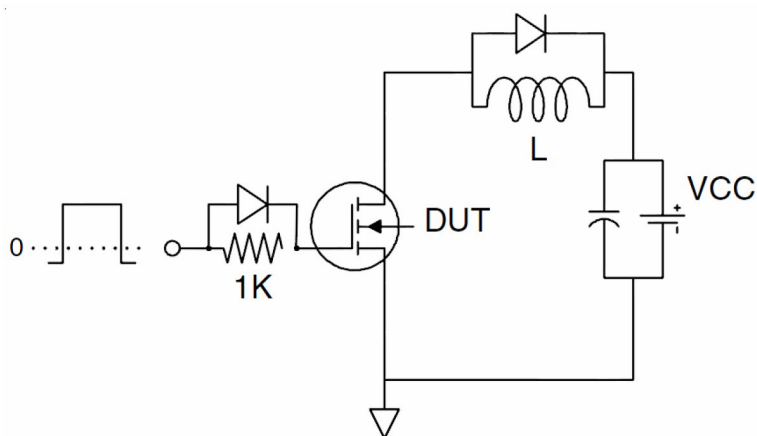
Notes:

- ① Surface Mounted on FR4 Board, t≤10sec.
- ② Pulse Test: Pulse Width≤400μs, Duty Cycle≤2%.
- ③ EAS condition：T_J=25°C,V_{DD}=37.5V,V_G=10V,L=2mH,R_g=25Ω,I_{AS}=37A
- ④ I_{SD}≤125A, di/dt≤260A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤175°C

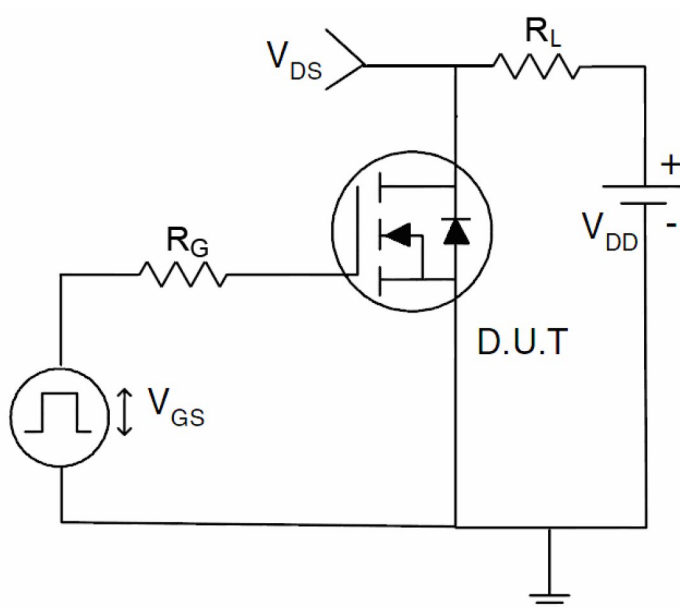
Test circuit



EAS test Circuit

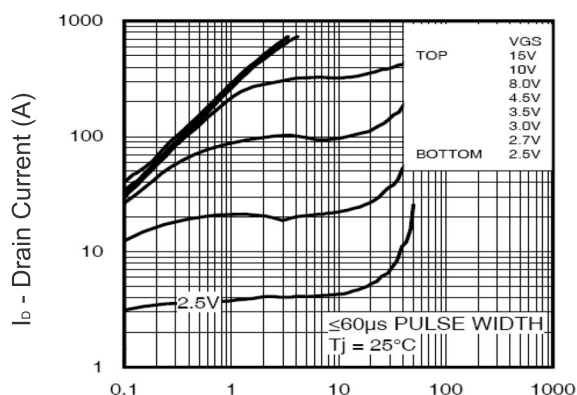


Gate charge test Circuit

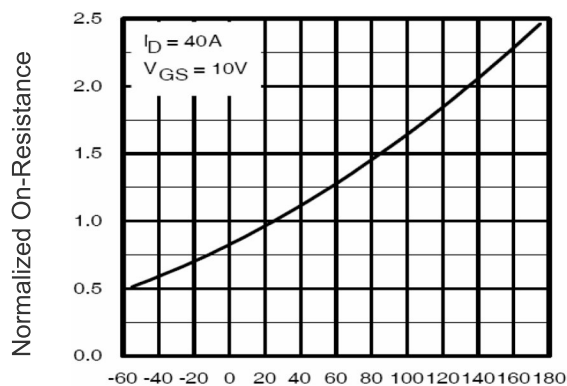


Switch Time Test Circuit

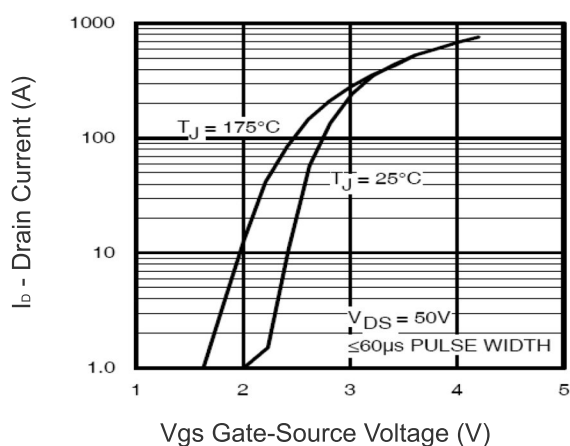
Typical Electrical and Thermal Characteristics (Curves)



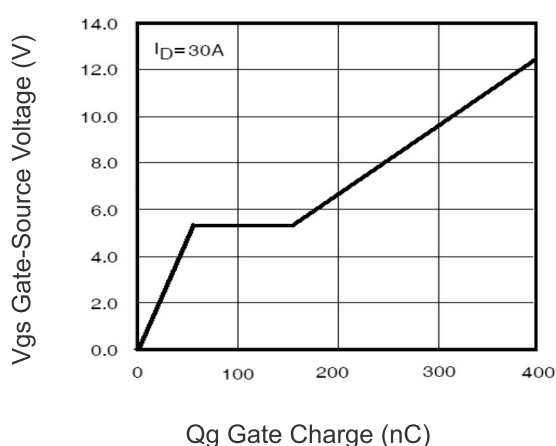
V_{DS} Drain-Source Voltage (V)
Figure 1 Output Characteristics



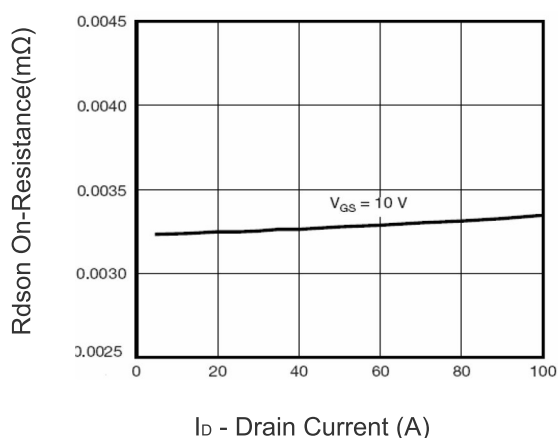
T_J -Junction Temperature(°C)
Figure 4 Rdson-Junction Temperature



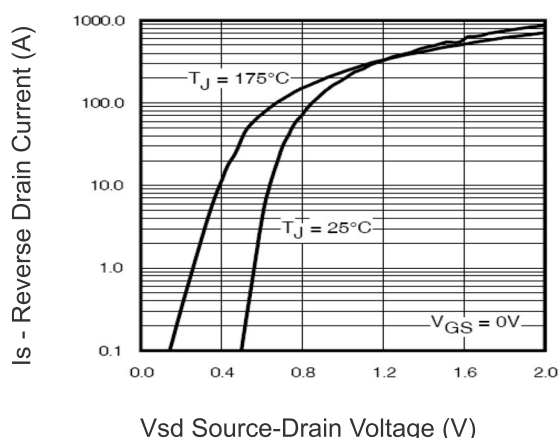
V_{GS} Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



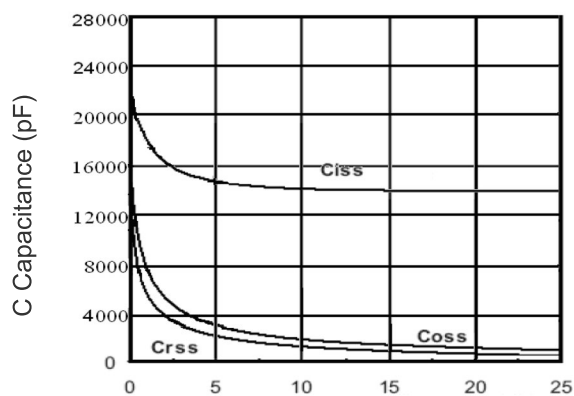
Q_g Gate Charge (nC)
Figure 5 Gate Charge



I_D - Drain Current (A)
Figure 3 Rdson- Drain Current

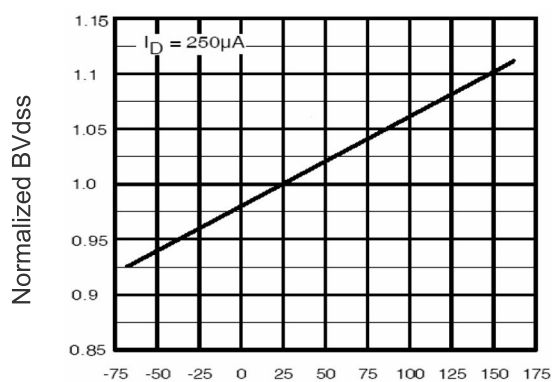


V_{SD} Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward

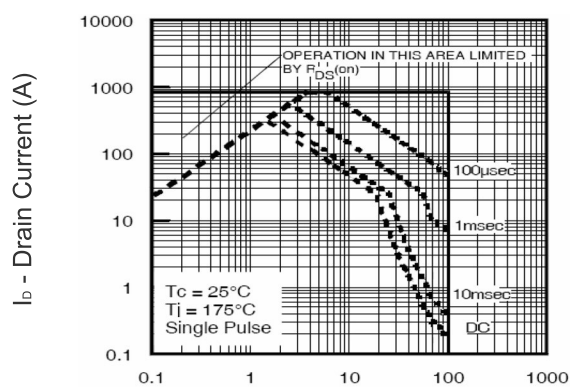


Vds Drain-Source Voltage (V)

Figure 7 Capacitance vs Vds

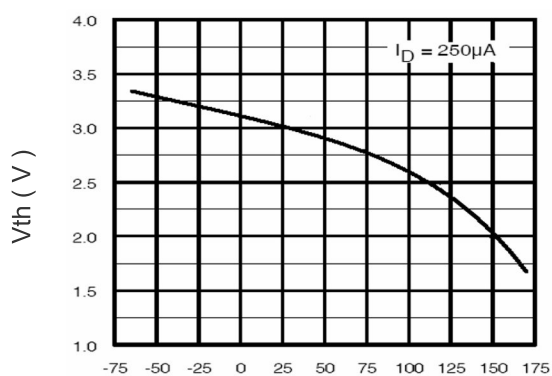


TJ -Junction Temperature(°C)

Figure 9 BV_{DSS} vs Junction Temperature


Vds Drain-Source Voltage (V)

Figure 8 Safe Operation Area



TJ -Junction Temperature(°C)

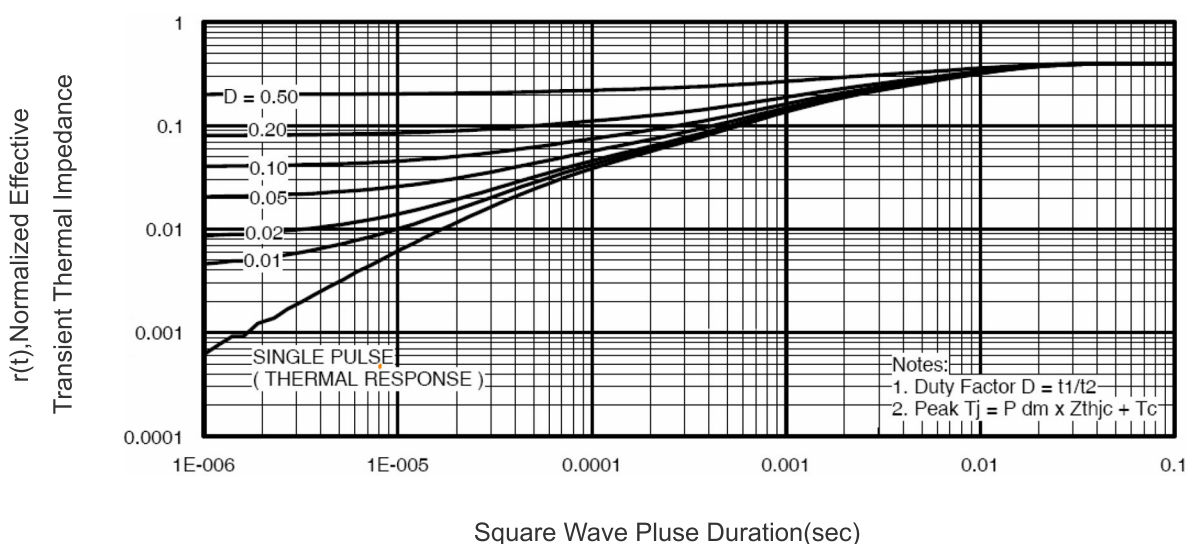
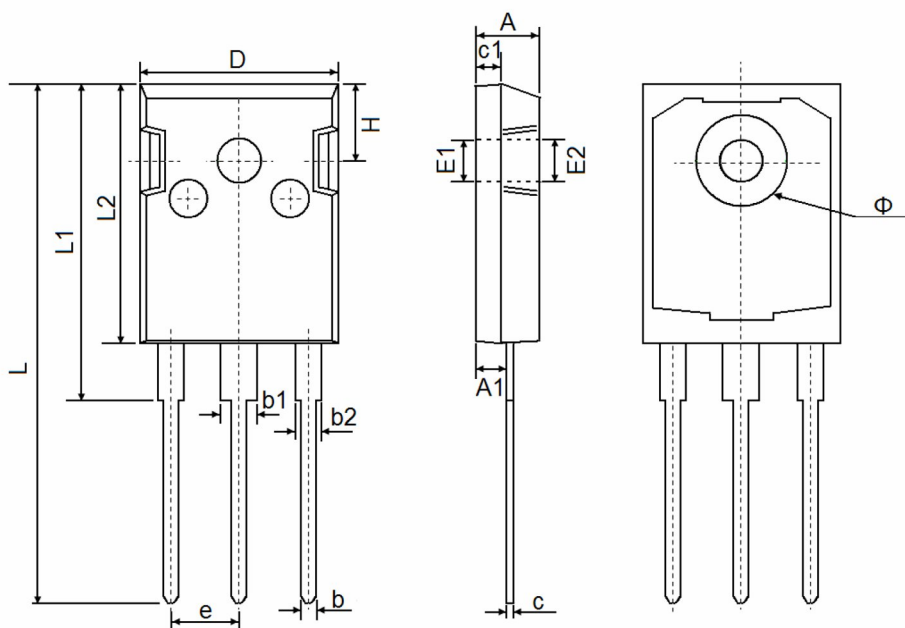
Figure 10 V_{GS(th)} vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-247 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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