MJ N-Channel Enhancement Mode Power MOSFET

Description

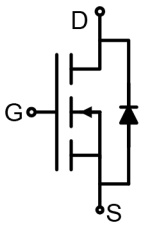
The MJ0102B uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

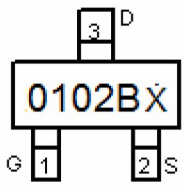
- V_{DS} =100V,I_D =1.8A
  $R_{DS(ON)}$ <680mΩ @ V_{GS} =10V
  $R_{DS(ON)}$ <700mΩ @ V_{GS} =4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin Assignment

SOT-23 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
0102B Ẋ	MJ0102B	SOT-23	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (T_C =25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{DS}	±20	V
Drain Current-Continuous	I_D	1.8	A
Pulsed Drain Current (Note 1)	I_{DM}	7.2	A
Maximum Power Dissipation	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J ,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	℃/W

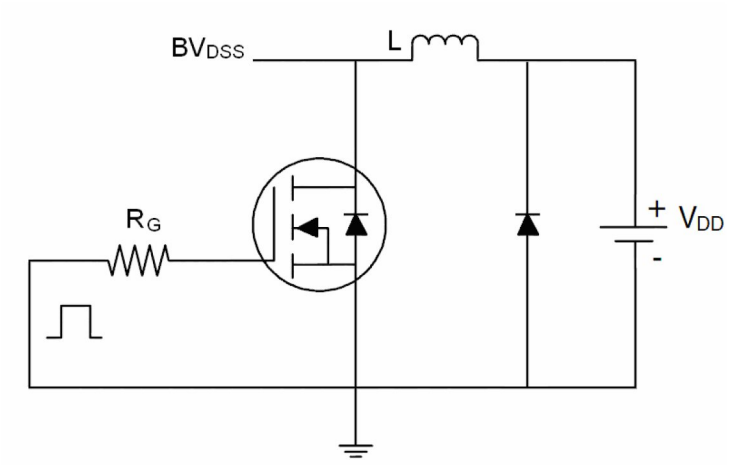
Electrical Characteristics (T_A =25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V I_D =-250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =100V,V_{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS} =±20V,V_{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS} ,I_D =250μA	1.2	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} =10V, I_D =1A	-	530	680	mΩ
		V_{GS} =4.5V, I_D =1A	-	580	700	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-5V,I_D =-5A	1	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{lss}	V_{DS} =50V,V_{GS} =0V, F=1.0MHz	-	164.6	-	PF
Output Capacitance	C_{oss}		-	11.5	-	PF
Reverse Transfer Capacitance	C_{rss}		-	6	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD} =30V, ,R_L =30Ω V_{GS} =10V,R_{GEN} =2.5Ω	-	5	-	nS
Turn-on Rise Time	t_r		-	4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	12	-	nS
Turn-Off Fall Time	t_f		-	5	-	nS
Total Gate Charge	Q_g	V_{DS} =50V,I_D =1A, V_{GS} =-10V	-	8.3		nC
Gate-Source Charge	Q_{gs}		-	1.7	-	nC
Gate-Drain Charge	Q_{gd}		-	1.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS} =0V,I_S =1A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	1.8	A

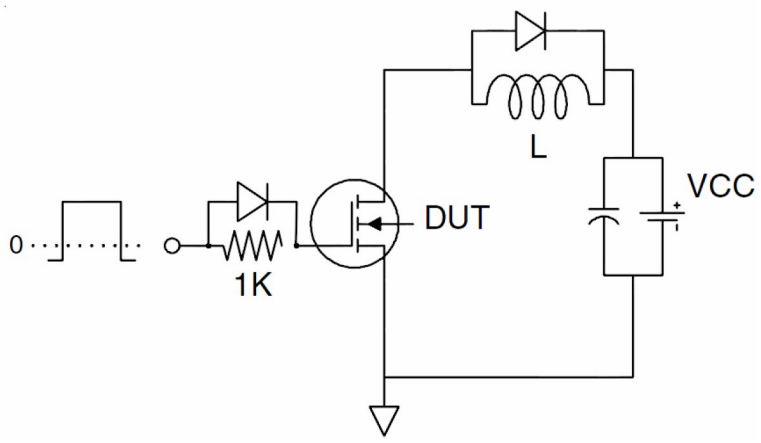
Notes:

① Repetitive Rating: Pulse width limited by maximum junction temperature.
② Surface Mounted on FR4 Board, t ≤ 10 sec.
③ Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
④ Guaranteed by design, not subject to production

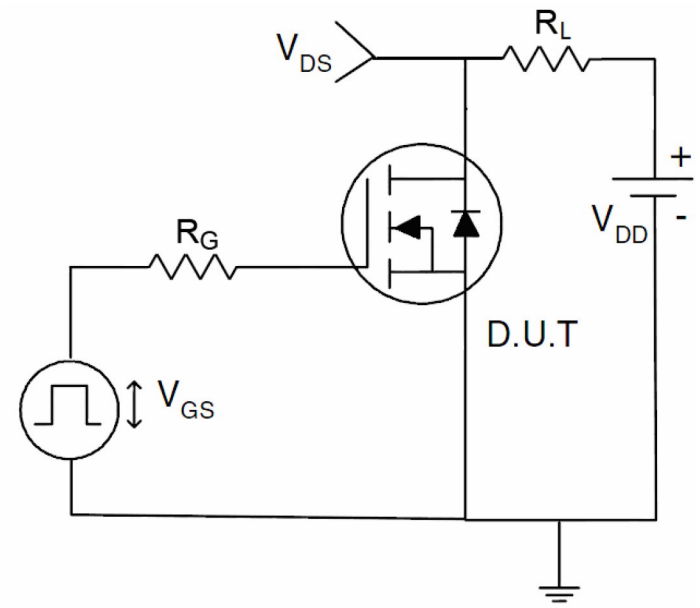
Test Circuit



EAS test Circuit



Gate charge test Circuit



Switch Time Test Circuit

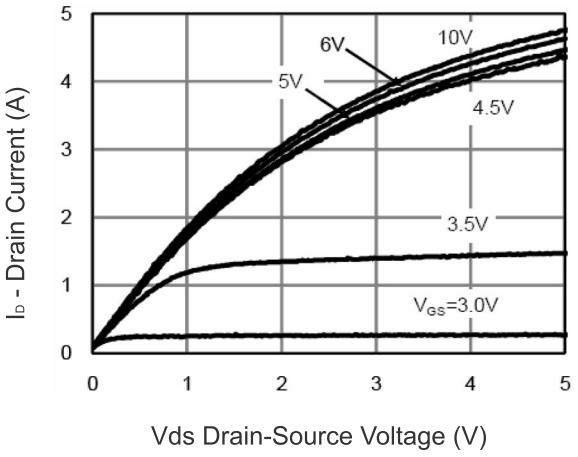


Figure 1 Output Characteristics

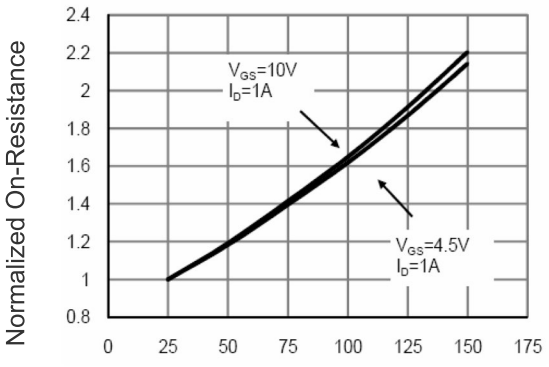


Figure 4 Rdson-Junction Temperature

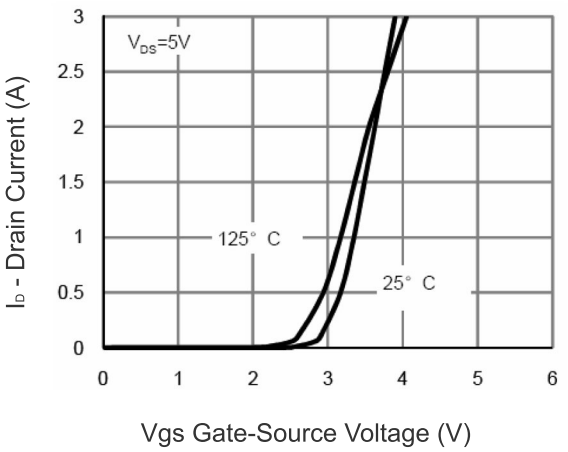


Figure 2 Transfer Characteristics

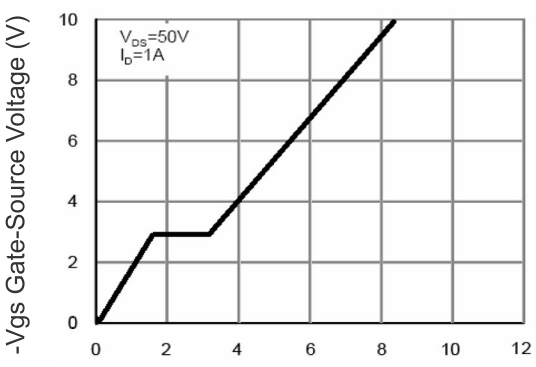


Figure 5 Gate Charge

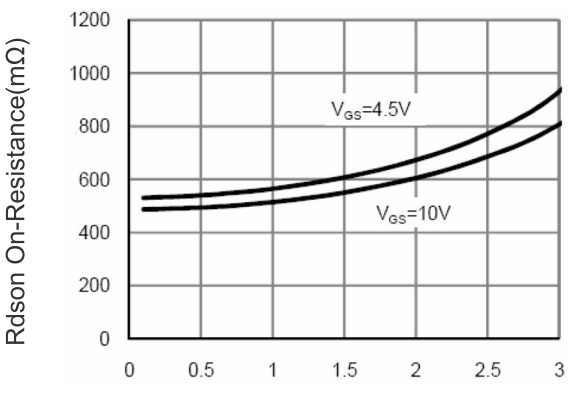


Figure 3 Rdson- Drain Current

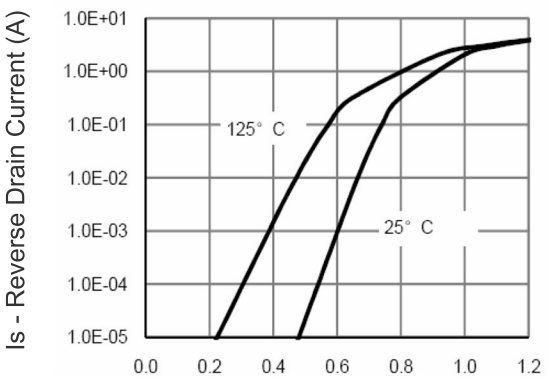


Figure 6 Source- Drain Diode Forward

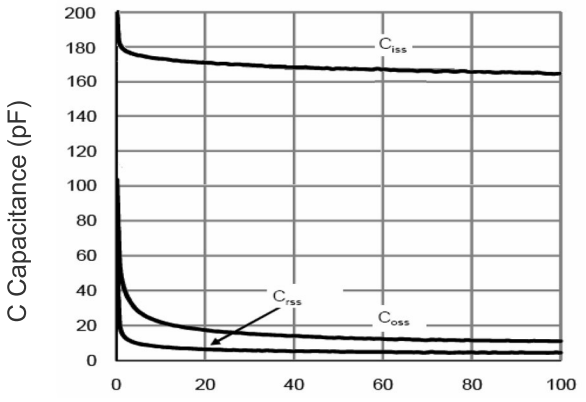


Figure 7 Capacitance vs Vds

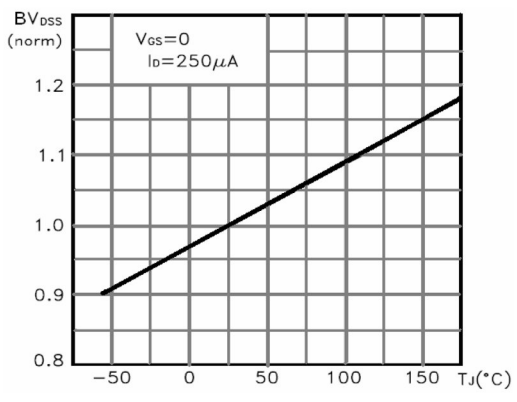


Figure 9 BV_{DSS} vs Junction Temperature

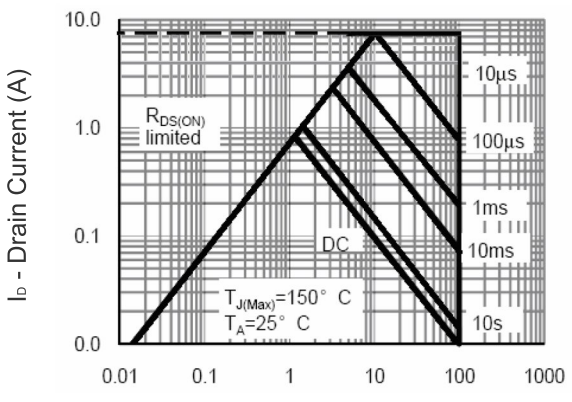


Figure 8 Safe Operation Area

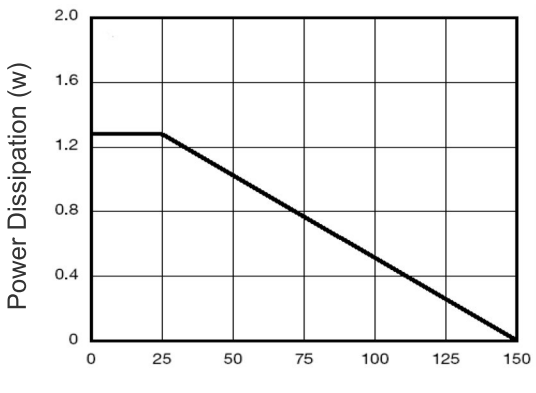


Figure 10 Power De-rating

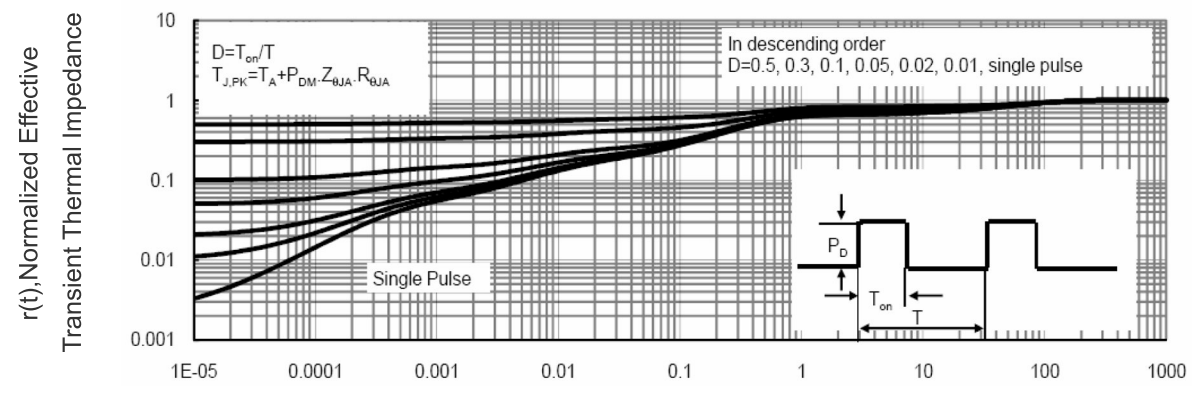
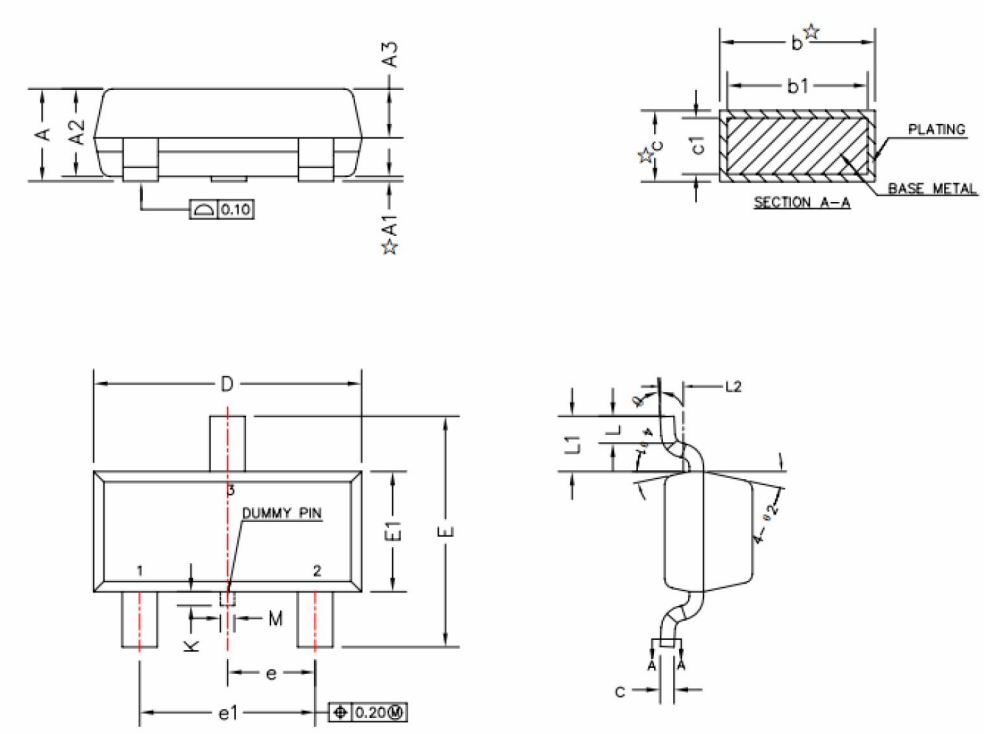


Figure 11 Normalized Maximum Transient Thermal Impedance

SOT-23-3L Package Information



Symbol	Millimeters	
	Min.	Max.
A	0.89	1.12
A1	0.01	0.10
A2	0.88	1.02
A3	0.43	0.63
b	0.36	0.50
b1	0.35	0.45
c	0.14	0.20
c1	0.14	0.16
D	2.80	3.00
E	2.35	2.64
E1	1.20	1.40
e	0.90	1.00
e1	1.80	2.00
L	0.40	0.60
L1	0.6REF	
L2	0.25BSC	
M	0.10	0.25
K	0.00	0.25
θ	0°	8°
θ1	10°	14°
θ2	10°	14°

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